MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 ELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 6

Issued: October 10, 2003 **Due:** October 17, 2003

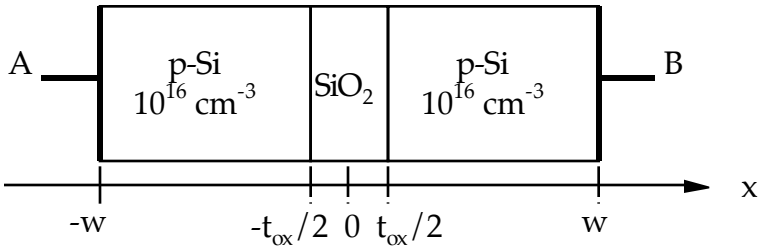
Reading Assignments:

Lecture 12 (10/14/03)- Chap. 10 (10.1.1a)
Lecture 13 (10/16/03)- Chap. 7 (7.2.2, 7.3.4); Chap. 8 (8.2.1); Chap. 10 (10.2.1)
Lecture 14 (10/21/03)- Chap. 7 (7.4.2); Chap. 8 (8.2.2, 8.2.3); Chap. 10 (10.2.2, 10.2.3)
Lecture 15 (10/23/03)- Chap. 15 (15.1, 15.2)
Lecture 16 (10/28/03)- Chap. 15 (15.2.4)

Problem 1 - Do Problem 9.1 in the course text using μ_h = 300 cm^2/V-s, rather than the value specified in the text.

Problem 2 - Do Problem 9.8 in the course text.

Problem 3 - This problem concerns the novel semiconductor-oxide-semiconductor (SOS) structure illustrated below. The two semiconductor regions are both p-type silicon with a net acceptor concentration of 10^{16} cm^{-3}; the oxide is a 50 nm (5 x 10^{-6} cm) thick layer of silicon dioxide. The dielectric constant of silicon, ε_{Si}, is 10^{-12} F/cm and of silicon dioxide, ε_{ox}, is 3.5 x 10^{-13} F/cm.



Use the depletion approximation model when solving this problem. Assume that the depletion region widths are less than w/2. The drawing may not be to scale.

(a) Sketch and label the electrostatic potential, $\psi(x)$, in this structure between -w/2 and +w/2 when $v_{AB} = 0$ and the structure is in thermal equilibrium.

(b) A bias is applied to this device sufficient to make the electrostatic potential at x = $t_{ox}/2$ equal to $-\phi_p$, where ϕ_p is the thermal equilibrium electrostatic potential in the p-type regions, i.e., $\psi(t_{ox}/2) = -\phi_p$. We call this the onset of inversion on the right side, and name this bias the right-side threshold, V_{TR}.

(i) What is the sign of V_{TR}? Explain your answer.
(ii) What is the width of the depletion region to the right of $x = t_{ox}/2$ with this applied bias?
(iii) What is the condition of the left-hand semiconductor-oxide interface, the one at $x = -t_{ox}/2$ with this applied bias?
(iv) What is the value of V_{TR}?

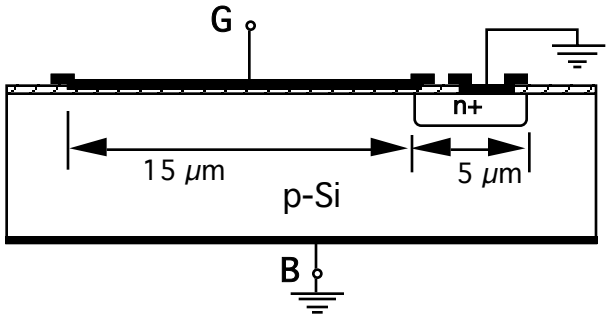
(c) Sketch and label the net charge density, $\rho(x)$, for $-w/2 < x < w/2$ when the bias voltage, V_{AB}, is V_{TR} + 2 Volts; recall V_{TR} was defined in Part (b). Be sure to label the vertical axis and to indicate the magnitude of any impulses (i.e., sheet charge densities).

(d) Define the left-hand threshold, V_{TL}, of the structure as the bias voltage, V_{AB}, at which the potential at $x = -t_{ox}/2$ is $-\phi_p$. What is V_{TL}? (You can give your answer in terms of V_{TR}, if you wish. Making use of symmetry should simplify your calculation.)

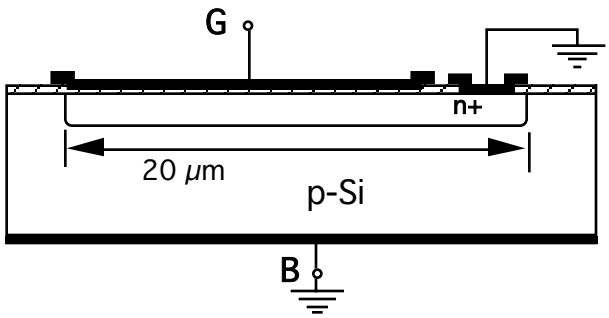
(e) Consider now a different SOS structure in which the left-hand semiconductor region is doped n-type, rather than p-type, with a net donor concentration of 10^{16} cm^{-3}.
(i) Sketch the electrostatic potential, $\phi(x)$ for $-w/2 < x < w/2$ in thermal equilibrium, i.e., $v_{AB} = 0$. Label the vertical axes but you do not calculate the widths of any depletion regions.
(ii) Sketch and label the electrostatic potential when v_{AB} is V_{TR} for this new structure, where V_{TR} has the same definition as before [see Part (b) above], but will not necessarily have the same value.
(iii) What is the value of V_{TL} for this new structure in terms of V_{TR} for this new structure, where V_{TR} and V_{TL} have the same definitions as earlier? (Making use of the antisymmetry of the problem will simplify your solution.)

Problem 4 - Consider the two silicon device structures shown in cross-section below:

Device A:



Device B:



Both of these devices are made on p-type silicon with a net doping level of 10^{17} cm^{-3}, and are 20 μm wide normal to the page. The n^+ regions are doped to 10^{18} cm^{-3}, and the n^+-p junction is 1 μm from the top surface. The thin oxide is a high quality thermal oxide 16 nm thick, and covers an area 20 μm wide by 15 μm long. In Device A the n^+ region is 20 μm wide by 5 μm long and extends just up to the edge of the thin

oxide, while in Device B it is 20 μm wide by 20 μm long and extends all the way under the thin oxide, as shown in the figure.

You may assume that throughout the silicon the electron mobility, μ_e, is 1600 $cm^2/V\text{-}s$ and the hole mobility, μ_h, is 600 $cm^2/V\text{-}s$ (except in an inversion layer in which case μ_e = 600 $cm^2/V\text{-}s$ and μ_h = 400 $cm^2/V\text{-}s$); that the intrinsic carrier concentration, n_i, is 10^{10} cm^{-3} at room temperature; and that the dielectric constant, ε_{Si}, is 10^{-12} F/cm. The dielectric constant of the oxide, ε_{ox}, is 3 x 10^{-13} F/cm, and the electrostatic potential of the gate metal relative to intrinsic Si is 0.3 V. (Note: There is more information here than you need, but we may add on to this problem in a later problem set.)

a) i) What is the electrostatic potential of the p-type silicon, relative to intrinisic silicon, in thermal equilibrium at room temperature?
ii) What is the built-in potential of the unbiased n+-p junction at room temperature?

b) What are the flat band voltages, V_{FB}, of the MOS capacitor structures in Devices A and B, respectively?

c) The <u>magnitude</u> of the threshold voltage, $|V_T|$, for the MOS structure is 1 V in one of these devices, and 4 V in the other. Use this information and your knowledge of MOS capacitors to deduce the <u>magnitude and sign</u> of V_T for each of these MOS capacitors, i.e., the one made on p-Si and the made on n+-Si.

d) What is the condition (accumulated, depleted, or inverted) of the semiconductor surface under the thin oxide in each of these devices with a gate voltage, V_{GB}, of 2 Volts? Also give the identity and sheet density of any mobile holes or electrons induced at the oxide-silicon interface.

<u>Problem 5</u> -This problem requires that you use a remote-control device measurement and characterization system called "weblab". Go to "http://weblab.mit.edu" and read the user manual provided there. (You were instructed to get a weblab user account on the last problem set, but if you did not do so and do not already have a user account, follow the instructions on Problem Set. 5). After reading the manual, make measurements on the device location 2 of weblab. You select the device that will be under test from the "Device" menu of the "Channel Definition" frame of the Java applet. The device is a p-n diode.

(a) Measure the current-voltage characteristic of this device between -10V and + 1 V. The maximum current the system will apply is 100 mA, and the devices can take this amount, but be gentle none the less. You have to exercise care with these devices. The p-n diode being measured is real and it can be damaged. If the characteristics look funny, try the second device and let us know (see final comments below).

Plot this characteristic two ways:
(i) on a linear scale, i.e. i_D vs v_{AB}, and
(ii) on a log-linear scale, i.e. log i_D vs v_{AB}.

Note that the "auto scale" function is very useful for displaying these plots. The lowest current that is meaningful on this instrument is 100 nA.

Finally, you should print out screen dumps of the "Measurements Results" frame of weblab and turn these in with the rest of your problem set solution.

(b) Compare the values of the satuation current, I_S, found by two methods:
(i) from $|i_D|$ for $v_{AB} << -kT/q$, and
(ii) from the intercept of $I_S e^{qv_{AB}/kT}$ on the vertical axis as v_{AB} goes to zero.

(c) From your log-linear plot determine the device temperature, assuming an ideal $e^{qv_{AB}/kT}$ variation. Notice that you have access to the actual data points from the "See Data" button of the "Measurements Results" frame. They can be downloaded to the local drive through the "Download Data" button.

(d) At what forward bias voltage does the assumption that one can ignore the series resistance in the quasi-neutral regions, contacts, and leads begin to fail? What do you estimate is the value of the series resistance in this device?

Additional final comments on weblab:

If you encounter problems with weblab or the diodes, please e-mail Prof. del Alamo, head of the weblab project (alamo@mit.edu), or the weblab system manager, Jim Hardison (hardison@mtl.mit.edu).

It will be to your advantage to make good use of the Set-up management functions that are built into the tool under the file menu of the "Channel Definition" panel (see user manual).

For research purposes, the system keeps a record of all logins and all scripts that each user executes.