Homework #1 - September 9, 2005

Due: September 16, 2005 at recitation (2 PM latest)
(late homework will not be accepted)

Please write your recitation session time on your problem set solution.

1. *[60 points]* A Dynamic Random Access Memory (DRAM) chip is composed of many cells that hold individual bits of information. For example, a 4 MB DRAM has about 4×10^6 cells where information can be held. At the heart of one of these cells is a capacitor that stores electrical charge. If the capacitor is charged, then we say that a "1" is stored. If the capacitor is discharged, then a "0" is stored. The smaller the capacitor, the denser the memory chip can be made. Achieving denser DRAM chips has been for the better part of the last 30 years a powerful technology driver for microelectronics, bringing along with it staggering progress in microprocessors and many other microelectronic products.

For a long time, the *minimum feature size*, or minimum dimension that can be reliably fabricated on a Si wafer, has been the bottleneck to high-density DRAM development. This is because the storage capacitor area is directly related to the minimum feature dimensions. As technology progressed and the minimum features size decreased, DRAM density increased. In the mid 90's, however, the situation changed dramatically. Rather than feature size, *dielectric breakdown* became a limiting phenomenom. This problem explores these issues.

This problem is designed to accomplish two goals:

1. to make you understand a few key issues in DRAM development: evolution, critical dimensions, limiting factors;

2. to make you review basic capacitor facts: charge, capacitance, field.

To a reasonable good approximation, a DRAM capacitor is basically a parallel plate capacitor where the insulator is made out of SiO_2 and the plates are made out of heavily-doped polycristalline Si. This, for all purposes, can be thought of as a metal, as you will come to understand soon in 6.012.

1. *[5 points]* Consider for a moment a 10 μm^2 area capacitor with a 30 nm thick SiO_2 dielectric. Compute the capacitance. The dielectric constant of SiO_2 is 3.9.
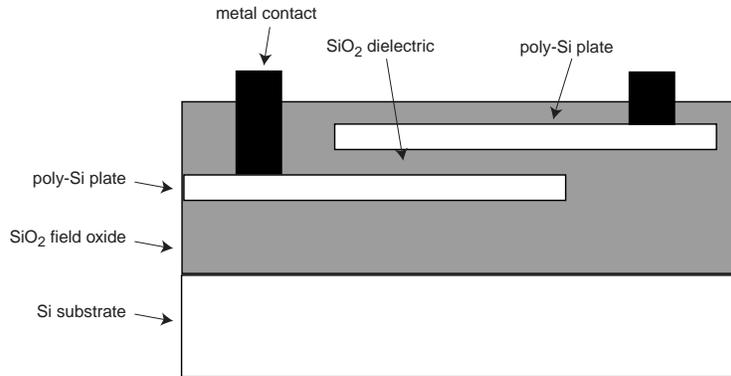
2. *[15 points]* With 4 *V* applied across this capacitor, *quantitatively* sketch the charge distribution, electric field, and electrostatic potential across the capacitor from plate to plate.

3. *[25 points]* Let's now look at the evolution of DRAMs. The following table contains the DRAM generation (4M, for example, means a DRAM with about four million bits), the year in which volume production started, and the minimum feature size used in that generation:

DRAM generation	year volume production	minimum feature size (μm)
1K	1972	4.6
4K	1974	3.2
16K	1977	2.4
64K	1980	1.8
256K	1983	1.5
1M	1986	1
4M	1989	0.8
16M	1992	0.5
64M	1995	0.35
256M	1998	0.25
1G	2001	0.18

Prepare a spreadsheet in which you compute the following items:

3a. *[5 points]* The *cell area*, A_c. This all-important parameter is intimately related to the minimum feature size. One cannot make a cell as small as the square of the minimum feature size. This is because in addition to the capacitor, there is a transistor, and interconnects in between. A historical average number for a parallel plate capacitor DRAM cell considered here is that the cell area is 16 times the square of the minimum feature size. One can call this factor of 16 a "cleverness factor" (the smaller it is, the more clever you are). Using a given feature size, the smarter you are in laying out and fabricating the cell, the

smaller it is going to be. Recent years have seen quite an improvement in this factor. In this problem, we will use a historical average value of 16.

3b. *[5 points]* The *capacitor storage area*, A_s. On average, for a parallel-plate capacitor DRAM cell, the capacitor area is about half of the cell area.

3c. *[5 points]* The *chip area*, A_{ch}. The chip also contains a lot more than just cells. It has, for example, busses, sense amplifiers, and input/output pads. So, to first order, the chip area is double the area of all cells combined.

3d. *[5 points]* The SiO_2 thickness, t_{ox}. For reasons of signal-to-noise ratio, the capacitance of DRAM cells has been essentially constant across generations. An average value is 40 fF. Based on this capacitance, compute the oxide thickness that each generation requires.

3e. *[5 points]* The electric field inside the insulator, $\mathcal{E}_{ox}$. Do this for two operating voltages, 5 V and 3.3 V. Consider that the actual voltage that is applied across the capacitor when a "1" is stored is 1 V smaller than the operating voltage. Do the calculation then for 4 V and 2.3 V.

4. *[5 points]* The maximum field that a material can withstand is called the *dielectric strength*, $\mathcal{E}_{br}$. For SiO_2, this field is 10^7 V/cm. If you exceed this value, dielectric breakdown takes place which results in lightning inside your capacitor! This is bad news for the cell. Based on your results, what is the densest DRAM generation that a parallel plate capacitor approach can produce for 5 V operation? How about 3.3 V operation?

5. *[5 points]* So, how to beat this limit? One approach that was investigated consisted of using an insulator with a higher dielectric constant. One that received considerable attention was Ta_2O_5. This material has a relative dielectric constant of 18 and a dielectric strength of 6 MV/cm. Rerun your spreadsheet for Ta_2O_5. What is now the densest DRAM generation that a parallel plate capacitor approach using Ta_2O_5 can produce for 5 V operation? How about 3.3 V operation?

6. *[5 points]* To even go beyond, one really has to make capacitors with an effective area that is bigger than the cell area. One can accomplish this by stacking smaller capacitors on top of each other, in what is known as a 3D design. Another way is to roughen up the surface of the plates to increase their effective area. Yet a third way is to bury the capacitor sideways into a trench that has been dug into the wafer. These trenches can be quite deep, as much as 10 μm. In all cases, you get a capacitor area that is bigger than the cell area.

To see what this approach entails, keeping the cell area as above, compute the capacitor area that makes possible a 1 Gb DRAM cell to operate at 3.3 V without suffering from dielectric breakdown. Consider both SiO_2 and Ta_2O_5 dielectrics.

2. *[40 points]* **I-V characteristics of pn diode**

Most of the homeworks in 6.012 this semester will include a small device characterization project. The goal of these projects is to expose students to real microelectronics devices: current-voltage characteristics, parameter extraction techniques, and model construction. These projects use the MIT Microelectronics WebLab, an online microelectronics device characterization test station that Prof. del Alamo and his students have been developing for a while in his lab at MIT. WebLab allows the educational use of professional microelectronics instrumentation by a large number of users through the internet.

Access to WebLab is provided through the MIT iLab Service Broker available at http://ilab.mit.edu. Your first step is to register by clicking on the *"register here"* tab. Then select admission in the *"OpenCourseWare Users"* group. Registration is not automatic but actually must be approved by the system manager. This typically takes less than a day but could take a few hours. You should therefore register early. Your one-stop shopping location for help, of any kind, regarding this assignment is through the *"Help"* tab in the iLab website. The WebLab team welcomes your feedback at *<ilab-debug@mit.edu>*. A manual for the use of this system is accessible from this site after logging in.

Engineers working at the cutting edge often use state-of-the-art design and simulation tools in their work. This is worthwhile even if it means dealing with a few bugs, small annoyances, and less than optimal documentation. WebLab 6.1 and the MIT iLab Service Broker are the latest generation in online microelectronic device characterization. In spite of extensive development and testing, it is possible that a few bugs remain. As engineers working at the state-of-the-art, you should approach this project in a conservative way and carry out your assignment as early as possible. You should also seek help if you find any difficulties.

In the device characterization assignments of 6.012, you will use an Agilent 4155B Semiconductor Parameter Analyzer. This professional tool allows you to obtain the current-voltage (I-V) characteristics of semiconductor devices.

In this first assignment, your task is to obtain, download and graph the I-V characteristics of a pn diode. In a follow-on assignment, you will attempt to fit a simple model to the measured characteristics. The pn diode is a device which basic behavior you have already studied in 6.002. One or more identical devices (labelled *pn Diode*) are available in WebLab under the *Devices* menu. The details of the device connection are available on-line. Do the following:

1) (*20 points*) Obtain I-V characteristics of the pn diode. Take measurements between -2 and 1 V. In the *measurement results panel* of WebLab, graph your results in the following way:

    graph 1: Linear plot of I-V characteristics (V in x axis in linear scale, I in y axis in

linear scale). Take a screen shot and print this graph. Turn in this graph.

graph 2: Semilogarithmic plot of I-V characteristics (V in x axis in linear scale, I in y axis in logarithmic scale). Note: in a logarithmic scale, weblab graphs the absolute of negative currents. Take a screen shot and print this graph. Turn in this graph.

You might need to go back and forth a few times trying different measurement point distributions so that sufficient data is taken in all regions of interest. Think also about issues involved in sweeping voltage vs. sweeping current. The maximum current the Agilent 4155B can support is 100 mA so for high voltages, the diode current will be clamped to 100 mA. The minimum current you should be concerned with is 1 pA.

2) (*20 points*) When you are happy with the results, download the data to your local machine and port them into your favorite spreadsheet program or MATLAB for graphing and analysis. Then do the following:

graph 3: Linear plot of I-V characteristics (V in x axis in linear scale, I in y axis in linear scale). Print out and turn in this graph.

graph 4: Semilogarithmic plot of I-V characteristics (V in x axis in linear scale, I in y axis in logarithmic scale). Note: in your spreadsheet program, you will have to compute the absolute of the current before you can graph it in a logarithmic scale. Print out and turn in this graph.

Turn in these four graphs and comment on how the measured I-V characteristics of the diode compare with those that you studied in 6.002.

Keep all the data handy as you will need them in a follow-on assignment in the next homework.

Additional information and assorted advice

- The required graphs 3 and 4 need not be too fancy, just simply correct and unambigous. They must have proper tickmarks, axis labelling, and correct units.

- You have to exercise care with this device. Please do not apply a higher voltage than suggested. The pn diode is real and it can be damaged. If the characteristics look funny, try one of the other devices and let us know.

- It will be to your advantage to make good use of the *Set-up* management functions that are built into the tool under the *File* menu.

- For research purposes, the system keeps a record of all logins and all scripts that each user executes.