Device Characterization and Circuit Design Project

Due **May 5, 2004** at 5pm (in 24-317 or at recitation)
Please write your recitation session time on your project report.

1 Introduction

In this project, you will characterize the current-voltage characteristics of an npn bipolar junction transistor (BJT) and an n-MOSFET. To do this, you will use the MIT Microelectronics WebLab.

The npn BJT is available in locations 4 and 5 of WebLab. It is labeled "npn BJT". The n-MOSFETs are in locations 6 and 7, labeled "nMOSFET (3 um)". This exercise involves three phases: (i) characterisation of the devices, large and small signal parameter extraction, (ii) using the measurements to choose bias voltages for a common collector amplifier to meet amplifier specifications, and (iii) using the measurements to determine small signal two port model parameters at the bias point.

Take the measurements specified below. When you are happy with the results (as judged by the characteristics displayed through the web), download the data to your local machine for more graphing and further analysis. You will find it useful to study the contents of Appendix A, which describes what the measured data should roughly look like and gives a short overview of the relevant equations.

The WebLab server is available at *http://ilabserv.mit.edu/ilab*

Important: Only hand in items for which you are asked. Do not hand in extra items, such as dumps of your measured data.

Late Policy: Late projects and projects handed in at wrong locations (i.e. not handed in at recitation or under the TA office door in 24-317) will only receive 50% of the normal grade. You are advised to measure the devices early. If you start only one or two days before the project is due, and for whatever reasons you cannot get your measurements done, you will not be granted an extension! While we try to fix problems (blown devices, etc.) as soon as possible, the response time may not be instant.

2 Design of common collector amplifier with NMOS current source

In this assignment you will characterize both an npn-BJT and an NMOS transistor, and use the measurements to design a common collector (emitter follower) amplifier with an NMOS current source, shown in Figure 1. In the design, you will choose the bias voltage V_B of the NMOS current source and the DC bias voltage, V_{BIAS}, in order to meet the following specs.

DC voltage gain	$A_{v0} > 0.95$
Input resistance	$R_{in} > 1$ MΩ
Output resistance	$R_{out} < 1$ kΩ
Voltage swing	$\geq \pm 1$ V about DC level
Supply voltage	$V_{DD} = 3$ V
DC Output voltage	$V_{OUT} = 1.5$ V

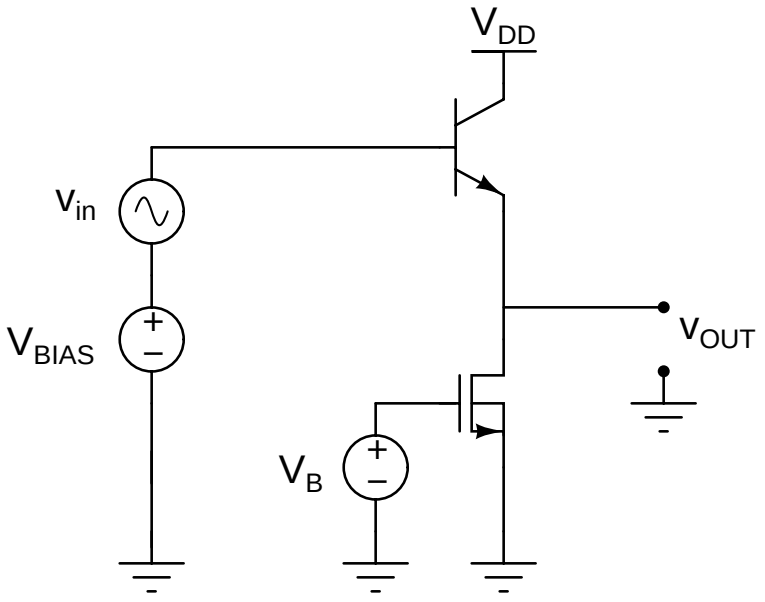


Figure 1: Schematic drawing of the common collector (also known as emitter follower) amplifier

3 Characterisation (*50 points total*)

1. (*20 points*) Obtain I-V characteristics for the BJT and the NMOS transistor. For the NMOS, use a maximum VDS and VGS of **3 Volts**. Measure I_D vs. V_{DS} with V_{GS} as a parameter. For the BJT, measure I_C vs. V_{CE} as a function of various $\mathbf{I_B}$ (not V_{BE}). You can find the range of I_B for the BJT characterisation by measuring the NMOS first. The range of I_B should be such that the resulting I_C is of the same order of magnitude as your measured I_D (since the amplifier operating point must have $I_D = I_C$). Also, to find g_m and r_π, measure I_C and I_B as a function of V_{BE}. Because of the exponential dependence, you must be careful with the value of V_{BE} you apply. Values above 0.9 V can damage the device! Look at your output characteristics for the BJT. If you also recorded V_{BE} in the measurements, you can get an idea of what values of V_{BE} to use. Do this measurement for various values of V_{CE}.

   Download the data onto your computer for use in Matlab or Excel. Show your measurement results in the following way:
   graph 1: output characteristics of the BJT, I_C vs. V_{CE}, for different values of I_B.
   graph 2: output characteristics of the NMOS, I_D vs. V_{DS}, for different values of V_{GS}.
   graph 3: for the BJT, plot I_C vs. V_{BE}, for different values of $V_{CE} > V_{CEsat}$.
   graph 4: for the BJT, plot I_B vs. V_{BE}, for different values of $V_{CE} > V_{CEsat}$.

   Note: Screen-shots of the Weblab measurements are not acceptable as graphs. Graphs must be **appropriately labelled** (by hand is okay) for full credit.

   Hand in: 4 graphs as specified

2. (*30 points*) So that you can select a bias point, you will need to graph some of the small signal parameters as a function of the bias point.
   graph 5: plot the output resistance (r_o) of the NMOS as a function of V_{DS}, for different values of I_D.
   graph 6: plot the output resistance (r_o) of the BJT as a function of V_{CE}, for different values of I_C.
   graph 7: for $V_{DS} = 1.5$ V, plot the output resistance (r_o) of the NMOS as a function of I_D.
   graph 8: for $V_{CE} = 1.5$ V, plot the output resistance (r_o) of the BJT as a function of I_C.
   graph 9: plot the transconductance (g_m) as a function of I_C, for $V_{CE} = 1.5$ V.
   graph 10: plot r_π of the BJT as a function of I_C for $V_{CE} = 1.5$ V.

   Hand in: 6 graphs as specified, appropriately labelled

4 Amplifier Design (*50 points total*)

1. (Small Signal - *30 points*) To help you determine the bias voltages, for the amplifier circuit of Figure 1, write down the equations for the DC voltage gain (A_{vo}) and the input and output resistances (R_{in}, R_{out}) in terms of the parameters derived from the measurements (g_m, r_{oBJT}, r_{oMOS}, r_π). Do not make simplifying assumptions (i.e. include effect of r_o)
   Take the requirements that the specs pose on A_{vo}, (R_{in}, R_{out} and the equations from above to solve for conditions that the specs pose on g_m, r_o, and r_π. For what range of $I_{SUP} = I_C = I_D$ do you meet the specs?

   Hand in: expressions as specified (show your work that leads to them or state where you found them), range of I_{SUP} that meets the specs.

2. (Bias point selectrion - *20 points*) Now that you have expressed the specs in terms of the measured small signal parameters and the requirements imposed on them, choose bias voltages V_B and V_{BIAS} that correspond to a point that meets the specs. Use the conditions you found in part 1. You will now also need to consider the voltage swing, V_{pp}. You can determine the swing by looking at r_{oMOS} vs. V_{DS} and r_{oBJT} vs. V_{CE} curves. The swing is met wherever the gain, input resistance, and output resistance specs are met. What device limits the up and down swing, and what physical effect causes the limitation?
   For your choice of bias voltages, find the measured small signal parameters and from there compute A_{vo}, R_{in}, R_{out} and V_{pp}.

   Hand in: the values for V_B and V_{BIAS}, the resulting A_{vo}, R_{in}, R_{out} and V_{pp}. State your reasoning that led to the choice of bias voltages, and an explanation of the upper and lower limitations of V_{pp}.

   Hint: If you cannot find bias conditions that meet the specs, re-meassure the devices around the bias point that meets the specs most closely. That way you have better resolution, since in your first measurements you may have measured so coarsely that the steps between the data are so large that you miss the working bias points.

5 Additional Information and Assorted Advice

The required graphs need not be too fancy, just simply correct. They must have proper tickmarks, axis labelling, and correct units. When there are several lines, each one should be clearly identified (handwriting is OK).

If you encounter problems with weblab or the devices, please use the "Report a Bug" link on the weblab website. Any message you report there will go to the system manager and to the weblab TA. If you have a conceptual or academic problem, e-mail the weblab TA, Wojtek (wpgiziew@mit.edu).

You have to exercise care with these devices. Please do not apply a higher voltage than suggested. The transistors are real and they can be damaged. If the characteristics look funny, try a different device and let us know. It will be to your advantage to make good use of the Set-up management functions that are built into the tool under the file menu of the channel definition panel (see manual).

For research purposes, the system keeps a record of all logins and all scripts that each user executes.

Note on collaboration policy

In carrying out this exercise (as in all exercises in this class), you may collaborate with somebody else that is taking the subject. In fact, collaboration is encouraged. However, this is not a group project to be divided among several participants. Every individual must have carried out the entire exercise, that means, using the web tool, graphing the data offline, and extracting suitable parameters. Everyone of these items contains a substantial educational experience that every individual must be exposed to. If you have questions regarding this policy, please ask the instructor. Prominently shown in your solutions should be the name of the person(s) you have collaborated with in this homework.

Appendix A - Definition of small signal parameters

MOS:

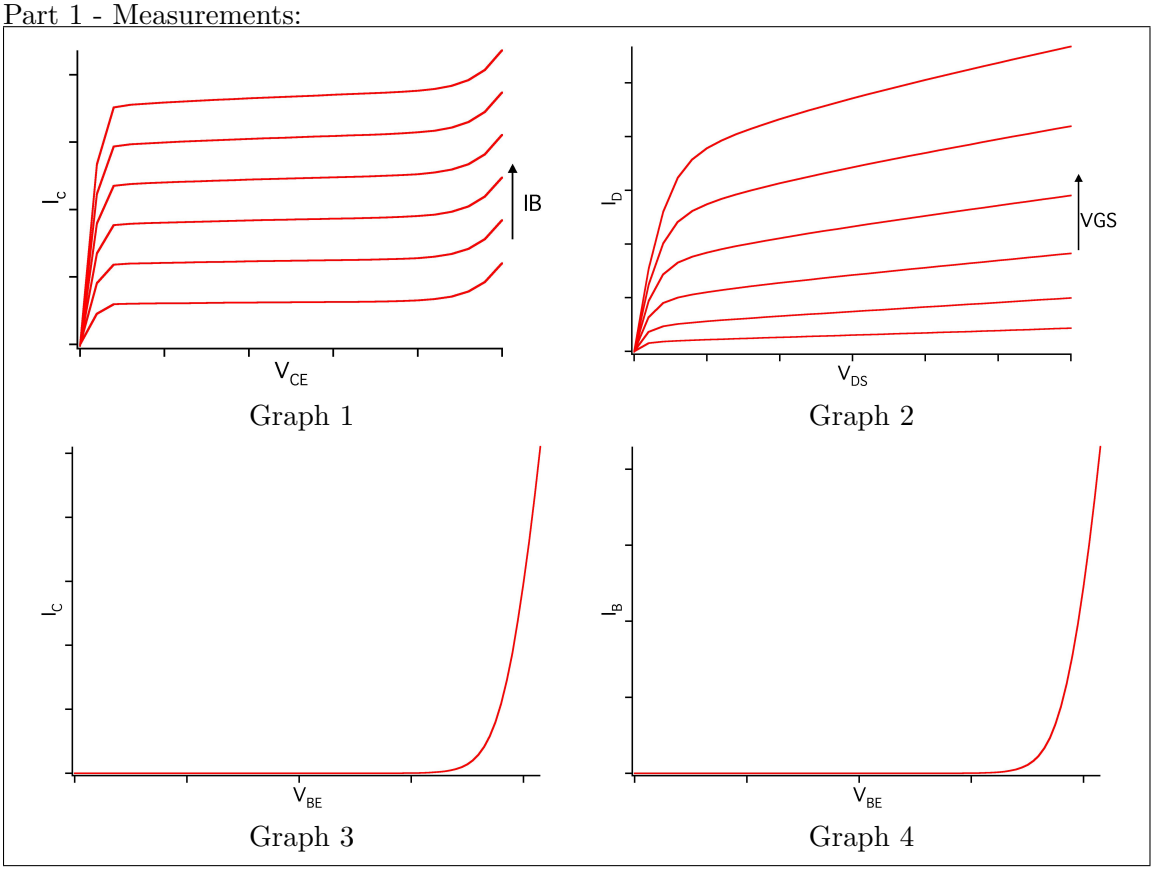
$$r_{oMOS} = \frac{1}{\frac{dI_D}{dV_{DS}}} \tag{1}$$

BJT:

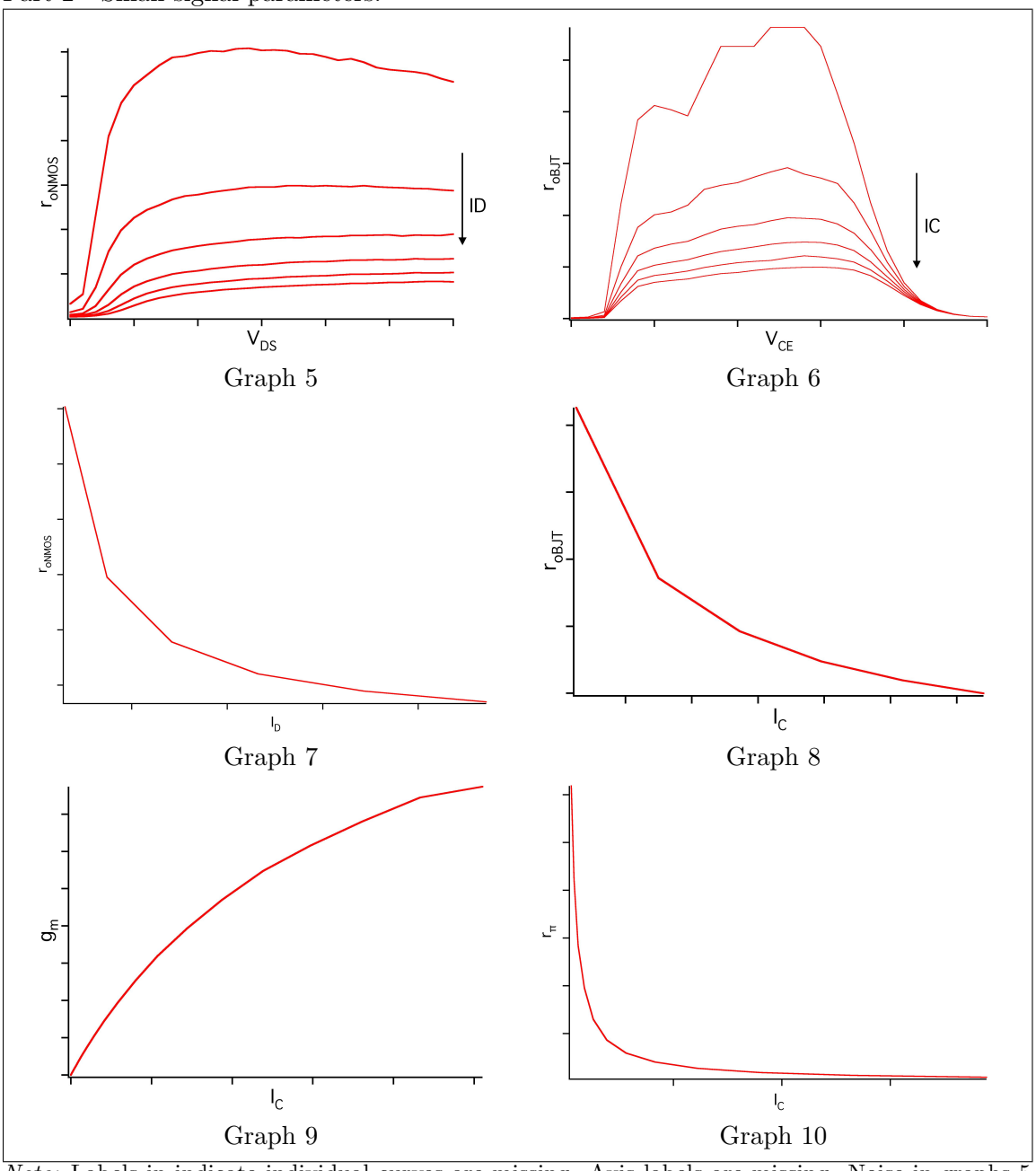
$$r_{oBJT} = \frac{1}{\frac{dI_C}{dV_{CE}}} \qquad r_\pi = \frac{1}{\frac{dI_B}{dV_{BE}}} \qquad g_m = \frac{dI_C}{dV_{BE}} \tag{2}$$

Appendix B - Typical Graphs

Part 1 - Measurements:



Part 2 - Small signal parameters:



Graph 5 Graph 6

Graph 7 Graph 8

Graph 9 Graph 10

Note: Labels in indicate individual curves are missing. Axis labels are missing. Noise in graphs 5 and 6 is due to using a simple, not smoothed, derivative.