Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Circuits & Electronics
Spring 2008

Problem Set #3

Issued 2/20/08 – Due 2/27/08

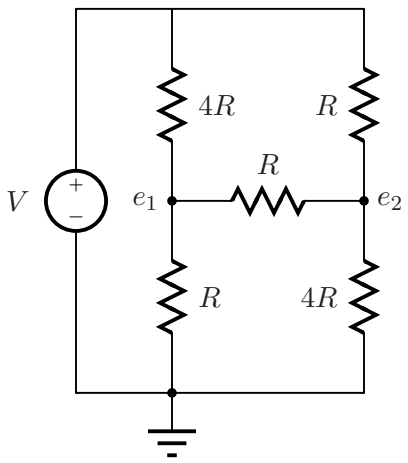
Exercise 3.1 (1 Point): An AA battery is measured to have an open-circuit voltage of 1.5 V, and a short-circuit current of 0.5 A. What would be the Thevenin and Norton equivalents of two such batteries connected in parallel, plus-to-plus and minus-to-minus? What is the maximum power that this battery combination can deliver to a load? What is the voltage across the load, and the current into it during maximum power delivery?

Exercise 3.2 (1 Point): This exercise applies two different analyses to determine the unknown node voltages e_1 and e_2 in Network A shown below. It illustrates that the direct method of analysis is not always the simplest.

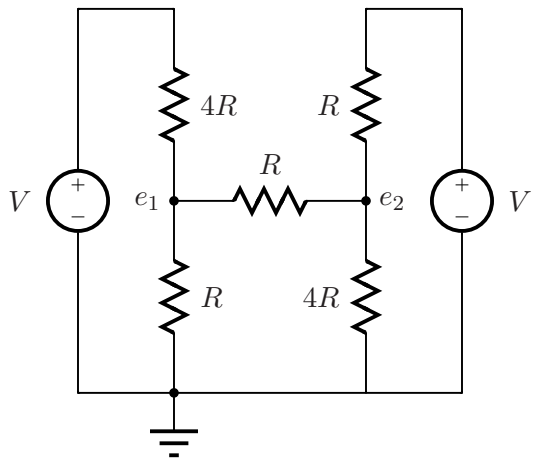
(A) Using nodal analysis, find the unknown node voltages in Network A. Hint: see Problem 1.3.

(B) First, explain why Network A may be re-drawn as Network B for the purpose of determining node voltages. Second, combine the left-hand source with the two left-most resistors to form their Thevenin equivalent, and redraw the resulting network. Third, combine the right-hand source with the two right-most resistors to form their Thevenin equivalent, and again redraw the resulting network. Finally, using superposition, determine the two unknown node voltages in the thrice re-drawn version of Network A thereby completing the analysis. Your answers to Parts A and B should be the same.

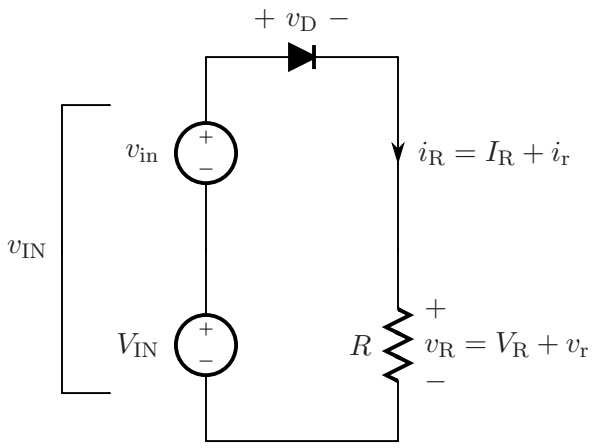
Network A



Network B



Problem 3.1 (2Points): This problem studies the small-signal characteristics of a network containing a non-linear diode, comparing experimental characteristics to those based on the theory developed in class. The network to be studied is the simple source-resistor-diode network shown below. The voltage source $v_{\rm IN}$ is shown in two parts: its large-signal bias $V_{\rm IN}$, and its small-signal variation $v_{\rm in}$. Correspondingly, the resistor current $i_{\rm R}$ and voltage $v_{\rm R}$ are expanded into their large-signal and small-signal components as well. This problem will study both the large-signal and small-signal characteristics of the network as a function of the input bias $V_{\rm IN}$, focusing in particular on the large-signal and small-signal components of $v_{\rm R}$.



This problem contains a theoretical component followed by an experimental component. The theoretical component involves model development, and the experimental component tests the predictions of the model. The experimental component will be carried out using the ELVIS iLab.

Consider first the behavior of the network from a theoretical viewpoint, using the methodology for small-signal analysis introduced in class. Here assume that the diode is ideal with a saturation current $I_{\rm S}$, and an operating temperature T.

(A) Assume that $I_{\rm R}$ is known. Derive expressions for $V_{\rm IN}$ and $V_{\rm R}$ in terms of $I_{\rm R}$, and the diode and resistor parameters. These expressions establish the biases within the network.

(B) Starting from the biases determined in Part (A), derive an expression for $v_{\rm r}$ in terms of $I_{\rm R}$, $v_{\rm in}$, and the diode and resistor parameters. In doing so, assume that $I_{\rm R}$ is so large that $I_{\rm R} \approx I_{\rm S}\ e^{(qV_{\rm D}/kT)}$.

(C) Rewrite the expression for $v_{\rm r}$ using $V_{\rm R}$ instead of $I_{\rm R}$ to represent the bias.

(D) Assume that $v_{\rm in}$ is 0.1 V, R is 10 kΩ, and the temperature kT/q is 26 mV. Using a calculator or a program of your choice, calculate v_r as a function of V_R for $V_{\rm R} = 0.1,\ 0.2,\ 0.3,\ 0.4$ and 0.5 V. Graph $v_{\rm r}$ as a function of $V_{\rm R}$.

You are now ready to carry out experiments to see the extent to which the results of Part (D) apply to a real network. To do so, you will use a new iLab called the ELVIS iLab. Thus, after logging in to iLab you must select and launch the *ELVIS Lab Client*. The ELVIS iLab is a versatile platform built by National Instruments that allows one to carry out simple experiments with circuits in the time domain.

When you launch the client, you will immediately see the network under test in the top half

of the GUI. It comprises the function generator *FGEN*, the diode, the 10-kΩ resistor, and the oscilloscope *SCOPE* that reads the voltage across the resistor. The diode is identical to the one that you characterized in Homework #2. To perform the experiments, you must suitably program the function generator and the oscilloscope as follows.

- First, double-click on the function generator. Set the WaveForm to *SINE*. Set the Frequency of the small signal $v_{\rm in}$ to 100 Hz, and its Amplitude to 100 mV. The Offset is the DC bias of the function generator, and corresponds to $V_{\rm IN}$. Run the first experiment with an Offset of 0.5 V. To save these settings, click *Apply* or *OK*.

- Next, double-click on the oscilloscope. Using its menu, set the sampling rate and the duration of the waveform to be acquired. You must think about appropriate settings for these two parameters. The sampling rate should be sufficiently greater than the frequency of the signal so that the signal can measured with good resolution. The duration is the time period over which the waveform will be acquired by the oscilloscope. The product of the sampling rate and the duration (plus one) is the total number of samples to be acquired, and this must be less than or equal to 2001. When you are ready with the settings, click *Apply* or *OK*.

- The experiment can now be run. Under the *Measurement* menu, click on *Run experiment*. If everything is properly configured, your experiment will now execute. If the queue is empty, the experiment will take about 20 seconds to execute. If you try to run your experiments at a very busy time, it might take much longer. Once the data comes back, the Y1 axis (the left vertical axis) will automatically display the input voltage $v_{\rm IN}$. You must program the Y2 axis (the right vertical axis) to display *VOUT* which is the total voltage $v_{\rm R}$ across the resistor. It will be easier if you leave the Y1 and Y2 axes in the *Autoscale* and *Linear* formats. From the results, you must read off the DC bias voltage across the resistor and the amplitude of the small-signal voltage across the resistor. To do so, you may wish to use the *Tracking* feature that the client offers at its bottom left. This feature allows you to read the coordinates of specific data points, or if you uncheck the *Snap to data points* box, the coordinates of any point on the canvas. To first order, you can assume that the bias in *VOUT* ($V_{\rm R}$) is the middle of its range, and that its peak small-signal amplitude (peak $v_{\rm r}$) is half of its peak-to-peak voltage difference.

- Carry out the experiment described above for the additional $V_{\rm IN}$ bias values of 0.4, 0.6, 0.7, 0.8, 0.9, and 1.0 V.

Now examine the experimental results as follows.

(E) Construct a table to display the results of your measurements. The table should have three columns. The first column should be the bias $V_{\rm IN}$. The second column should be the bias $V_{\rm R}$. The third column should be the peak amplitude of $v_{\rm r}$, which corresponds to $v_{\rm in} = 0.1$ V. Notice that the bias and small-signal amplitude of $v_{\rm IN}$ that you read from the canvas will not be exactly the same as those set in the function generator. The function generator is not very precise. Therefore, if you want to use information about $v_{\rm IN}$, you should read it directly from the canvas. Record your measurements in the table.

(F) Graph the small-signal peak amplitude of the experimental $v_{\rm r}$ against the bias $v_{\rm R}$ on the same graph that you constructed above using the model. Comment on the results that you obtain.

Problem 3.2 (2Points): The switch-resistor (SR) model of a MOSFET is a highly simplified model that is nonetheless very useful for describing the behavior of a MOSFET in a digital logic circuit. However, this model is so simplified that it can lead to inconsistent analyses in some cases, as illustrated by this problem.

Consider the analysis of the two-input NAND and two-input NOR gates shown below. Assume that all MOSFETS in these gates behave according to the SR model with a threshold voltage $V_T = 1$ V, and on-state resistance R_{ON}. Further, let $R_{PU} = R_{ON}$, and $V_S = 3$ V.

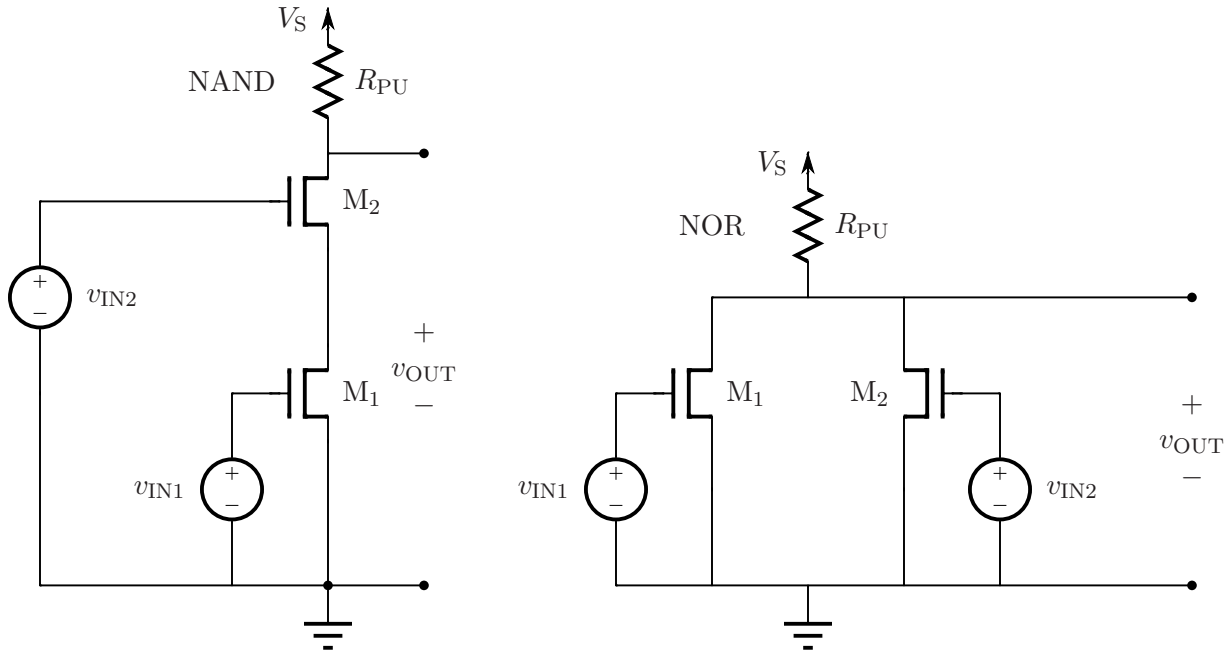
(A) Consider the two-input NAND gate. Let $v_{IN1} = v_{IN2} = 1.5$ V. Assume that M_2 is on and determine v_{OUT} and v_{GS} for M_2. (Is M_1 on or off?) Is the value of v_{GS} consistent with the assumption that M_2 is on?

(B) Again consider the two-input NAND gate, and again let $v_{IN1} = v_{IN2} = 1.5$ V. Now assume that M_2 is off and determine v_{OUT} and v_{GS} for M_2. Is the value of v_{GS} consistent with the assumption that M_2 is off?

(C) From your answers to Parts (A) and (B) you should conclude that M_2 can be neither on nor off. What characteristics of the SR model and the design of the two-input NAND gate allow this inconsistency to occur? How do you think the real circuit actually behaves?

(D) How high must V_{IH} be defined for the two-input NAND gate so that the inconsistent analysis found above is inconsequential to the proper operation of the gate?

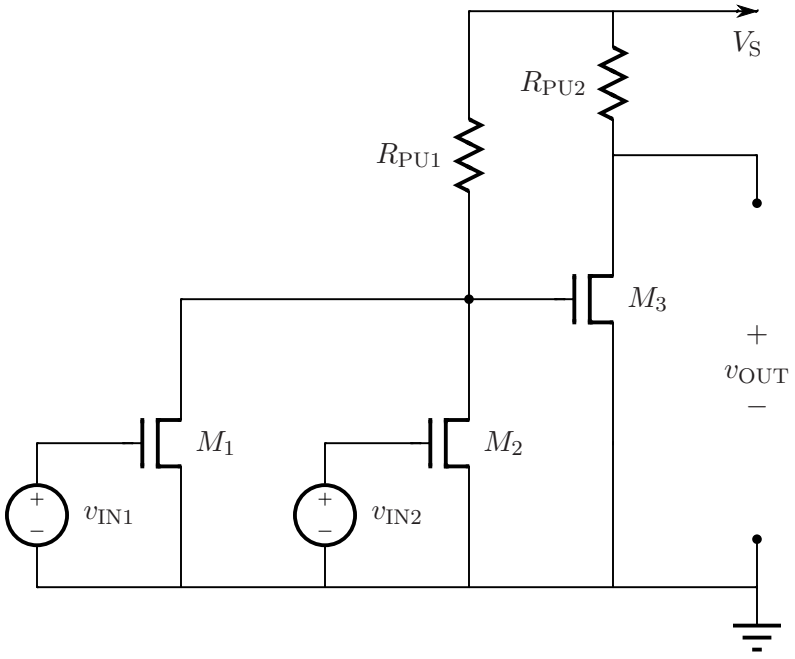
(E) Consider now the two-input NOR gate. Can its analysis produce the same inconsistency for any combination of parameter values? Why or why not?



Problem 3.3 (2 Points): Consider the NMOS two-input OR gate shown below. This gate is to be implemented with MOSFETs having 0.5 V $\leq V_{\rm T} \leq$ 4 V and $10^3\ \Omega \leq R_{\rm ON} \leq 10^5\ \Omega$, and pull-up resistors having $10^3\ \Omega \leq R_{\rm PU} \leq 10^5\ \Omega$. (The inequalities express a permissible design space as opposed to a range of manufacturing uncertainty.) The MOSFETs and pull-up resistors need not have identical parameters.

(A) Complete the design of the OR gate by choosing values for each $V_{\rm T}$, $R_{\rm ON}$ and $R_{\rm PU}$ so that: $V_{\rm OL} = 1$ V; $V_{\rm IL} = 2$ V; $V_{\rm IH} = 3$ V; $V_{\rm OH} = 4$ V; and the power dissipated by the gate is minimized. If any parameter does not have a unique design value, then give the permissible range for that parameter. Assume $V_{\rm S} = 5$V.

(B) Let all $R_{\rm PU}$ and $R_{\rm ON}$ be 10 kΩ. Assume that all $V_{\rm T}$ are chosen so that the circuit works properly as a two-input OR gate. Determine the average power dissipated in the circuit for the case in which all logical input combinations are equally likely over time.



Problem 3.4 (2 Points): This problem makes use of the Microelectronics Device Characterization Laboratory iLab to measure the voltage-current characteristics of a MOSFET. There are two standard ways to display the current-voltage characteristics of a MOSFET. The first is called the *output characteristics*. The second is called the *transfer characteristics*. In this problem you will explore them both.

The output characteristics of a MOSFET refer to a graph displaying the drain current $i_{\rm D}$ as a function of the drain-to-source voltage $v_{\rm DS}$, with the gate-to-source voltage $v_{\rm GS}$ acting as a parameter. Use the following procedure to obtain the output characteristics of the 2N7000 MOSFET.

- As in earlier problems involving this iLab, login to iLab, select the *Microelectronics Device Characterization Lab Client V7.0* and launch it. Then select the 2N7000 MOSFET under the *Device menu*. This is the device that you will characterize.
- For all measurements, the MOSFET source should be grounded. To do so, select its SMU and

set MODE to COMM. Name the variables, but do not select them for downloading.

- The MOSFET drain voltage should be set to sweep over an inner loop. To do so, select its SMU and then set: MODE = V, FUNCTION = VAR1, Scale = Linear, and COMPLIANCE = 100 mA. Set VAR1 to sweep from 0 V to 5 V in 200-mV steps. Name both variables and select both for downloading. These variables are v_{DS} and i_{D}.

- The MOSFET gate voltage should be set to sweep over an outer loop. To do so, select its SMU and set: MODE = V, FUNCTION = VAR2, Scale = Linear, and COMPLIANCE = 100 mA. Set VAR2 to sweep from 1.9 V to 2.5 V in 100-mV steps. Name both variables but do not select them for downloading.

- Execute the experiment to measure the MOSFET output characteristics.

(A) Plot the measured characteristics with v_{DS} on the horizontal axis over the range 0 V to 5 V, and i_{D} on the vertical axis over the range 0 mA to 10 mA. Both should be on linear scales. You can do so directly with iLab and then capture a screen shot for printing. Alternatively, you can download the measurements, and then plot and print them using another program such as MatLab or Excel. Note that the measured data will not all fit within the specified graphing range.

The transfer characteristics of a MOSFET refer to a graph displaying the drain current i_{D} as a function of the gate-to-source voltage v_{GS}, with the drain-to-source voltage v_{DS} acting as a parameter. Use the following procedure to obtain the transfer characteristics of the 2N7000 MOSFET.

- Again, ground the MOSFET source.

- The gate voltage should be set to sweep over an inner loop. To do so, select its SMU and set: MODE = V, FUNCTION = VAR1, Scale = Linear, and COMPLIANCE = 100 mA. Set VAR1 to sweep from 0 V to 3 V in 50-mV steps. Name both variables and select the gate voltage v_{GS} for downloading.

- The drain voltage should be set at the fixed voltage of 4 V. To do so, select its SMU and set: MODE = CONS and VALUE = 4 V. The COMPLIANCE should be set to 100 mA. Name both variables and select the drain current, i_{D}, for downloading.

- Execute your program to measure the MOSFET characteristics.

(B) Plot the measured characteristics with v_{GS} on the horizontal axis over the range 0 V to 3 V, and i_{D} on the vertical axis over the range 0 mA to 10 mA.

(C) Based on the data that you obtained in Parts (A) and (B), determine the threshold voltage V_T of the MOSFET.

(D) Over what region of v_{DS} and v_{GS} does the MOSFET behave as a reasonable switch? In the sub-region in which the switch is closed, what is a suitable value for the on-state resistance R_{ON} of the MOSFET? Again, base your answer on the data that you obtained in Parts (A) and (B).