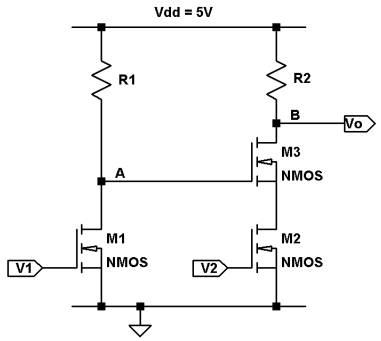
Homework # 5 Solution

Due: Never

1. *[20 Points]*: For part (a) to (c), all MOSFETs have the same $V_T = 2V$ and $K = 0.1mA/V^2$. The input voltages V_1 and V_2 represent logic values: 0 (V_1 or V_2 <1V) and 1 (V_1 or V_2 > 3V). The power supply is $V_{dd} = 5V$.



(a) *[4 Points]* What should be the value of R_1 so that the noise margin at node A is 0.5V?
Noise margin (NM_0) is defined as the largest amount of noise that can be added to any valid output (V_O) before it becomes invalid as the input (V_I) for the next stage.
I.e. $NM_0 = Min(|V_{IL}-V_{OL}|, |V_{OH}-V_{IH}|)$

Answer:
Given $V_{IL} = 1V$, $V_{IH} = 3V$, and noise margin $NM_0 = 0.5V$, we know
$V_{OL} = 0.5V$, $V_{OH} = 3.5V$

When V_1 is low, M1 is off,
$V_A = 5V > 3.5V = V_{OH}$

When $V_1 = 3V$ (worse case), M1 is on, notice
$V_{OL} = 0.5V < V_1 - V_T = 1V$, in triode,
$V_A = V_{dd} - I_{D1}R_1$
$= V_{dd} - K*V_A*(V_1 - V_T - V_A/2)*R_1$
$= 5 - 0.1m*V_A*(1 - V_A/2)*R_1$
Also,
$V_A < V_{OL} = 0.5V$

Therefore,
$R_1 > 120k\Omega$

(b) *[4 Points]* Assume now for simplicity that when "ON" these MOSFETs can be represented by a resistance $R_{ON} = 5k\Omega$. What should be the value of R_2 so that the noise margin at node B is 0.5V?

Answer:
From (a), we know $V_{OL} = 0.5V$, $V_{OH} = 3.5V$.

When M2 is off,
$V_B = 5V > 3.5V = V_{OH}$

When M2 is on,
$V_B = V_{dd}*2R_{ON}/(2R_{ON}+R_2) < V_{OL} = 0.5V$

Thus,
$R_2 > 90k\Omega$

(c) *[4 Points]* What logic function is implemented?

Answer:

V_1	V_2	V_O
0	0	1
0	1	0
1	0	1
1	0	1

$V_O = \neg(\neg V_1 * V_2) = V_1 + (\neg V_2)$

(d) *[8 Points]* Consider now that this gate is to be implemented with MOSFETs having $0.5V < V_T < 3V$ and $10^3\Omega < R_{ON} < 10^5\Omega$, and pull-up resistors having $10^3\Omega < R_{PU} < 10^5\Omega$. (The inequalities express a permissible design space as opposed to a range of manufacturing uncertainty.) The MOSFETs and pull-up resistors need not have identical parameters.

Complete the design of the logic gate by choosing values of V_T and R_{ON} for each transistor, and R_{PU1} and R_{PU2} so that: $V_{OL} = 0.5V$; $V_{IL} = 1.5V$; $V_{IH} = 2V$; $V_{OH} = 3V$; and the power dissipated by the gate is minimized. If any parameter does not have a unique design value, then give the permissible range for that parameter. Assume $V_{dd} = 5V$.

Answer:
For all MOSFETs,

$$V_{IL} < V_T < V_{IH}$$

Thus,

$$1.5V < V_T < 2V$$

To minimize power dissipation, we choose the largest possible R_{PU}'s for both pull-up resistors,

$$R_1 = R_2 = R_{PU} = 10^5\Omega$$

To satisfy $V_{OL} = 0.5V$, when M1 is on,

$$V_A = V_{dd}*R_{ON1}/(R_{ON1}+R_1) < V_{OL} = 0.5V$$

Thus,

$$R_{ON1} < 11k\Omega$$

Similarly,

$$V_B = V_{dd}*(R_{ON2}+R_{ON3})/(R_{ON2}+R_{ON3}+R_2) < V_{OL} = 0.5V$$

$$R_{ON2}+R_{ON3} < 11k\Omega$$

(Note: Strictly speaking, one should choose $R_{ON1} = 11k\Omega$ and $R_{ON2}+R_{ON3} = 11k\Omega$, in order to minimize power dissipation. However, given R_{ON} is usually much smaller than R_{PU}, in most cases, power dissipation is dominated by R_{PU}. Therefore, we care less about the exact value of R_{ON}. Moreover, in practice, R_{ON} is a function of V_{GS}, and also process dependent, which makes absolute value of R_{ON} very hard to control.)

2. *[20 Points]*: For all parts below, assume the input is a step signal, and zero initial condition:

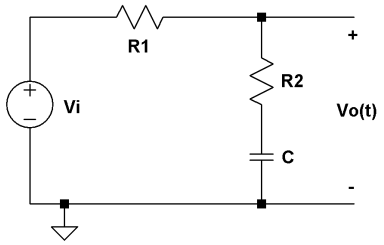
$$v_I(t) = \begin{cases} 0 & t < 0 \\ V & t > 0 \end{cases}$$

In addition, assume the capacitor voltage at t=0 is zero:

$$v_C(t=0) = 0.$$

Calculate the time constant(s); sketch and label carefully $v_O(t)$.

(a) *[5 Points]*

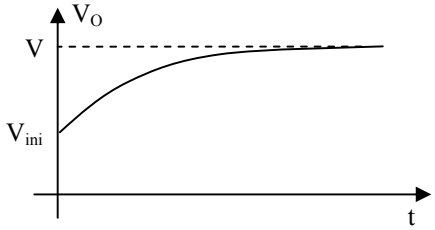


Answer:

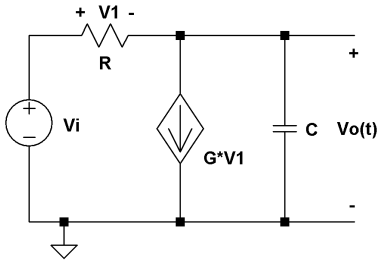
$v_O(t=0^+) = V*R_2/(R_1+R_2) = V_{ini}$

$v_O(t=\infty) = V$

$\tau = (R_1+R_2)C$



(b) *[5 Points]* Assume G < 1/R.

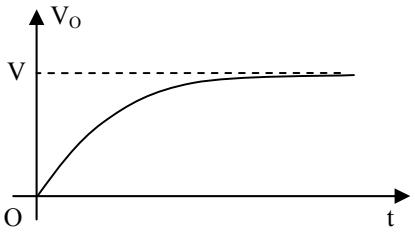


Answer:

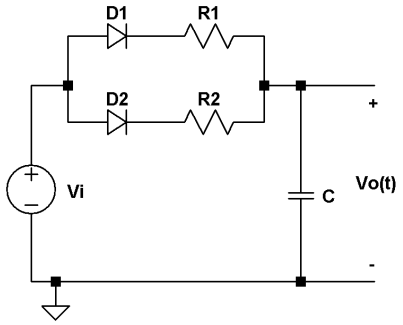
$v_O(t=0^+) = 0$

$v_O(t=\infty) = V$

$\tau = RC/(1-RG)$



(c) *[5 Points]* Assume the diodes are ideal.

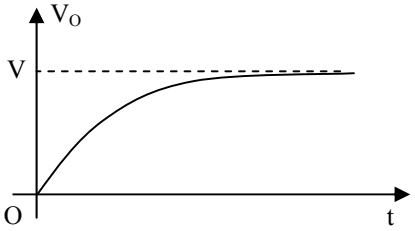


Answer:

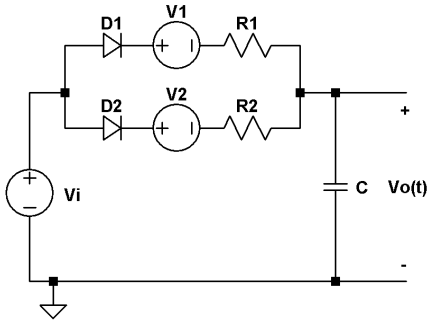
$v_O(t=0^+) = 0$

$v_O(t=\infty) = V$

$\tau = (R_1 \| R_2)C$



(d) *[5 Points]* Assume the diodes are ideal, and $V_1 = V_X$, $V_2 = 2V_X$. ($V_2 < V$)



Answer:

$v_O(t=0^+) = 0$

When $V_O < V - 2V_X$, both diodes are on, V_O increases with a time constant τ_1,

$$\tau_1 = (R_1 \| R_2)C$$

targeting at a final value

$$V_{f1} = V$$

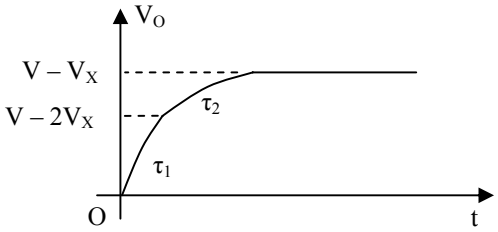
When $V - 2V_X < V_O < V - V_X$, D1 is on, D2 is off, VO continues to increase with a time constant τ_2,

$$\tau_2 = R_1 C$$

targeting at a final value

$$V_{f2} = V$$

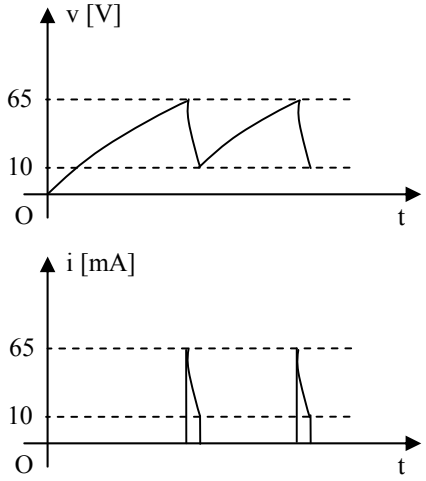
When V_O reaches $V - V_X$, both diodes turn off. V_O is not going to change any more.



3. *[20 Points]*: Agarwal and Lang, Problem 10.22 (Assume zero initial state, $v_C(t=0) = 0$)

Answer:

(a)



(b) When $v(t) < V_T = 65V$, the neon bulb acts as an open circuit, the capacitor is charging up, with a time constant τ_1,

$$\tau_1 = RC = 10s$$

targeting at a final value

$$V_{f1} = 90V$$

Once v(t) reaches V_T, the bulb begins to discharge. Notice $R_N << R$, so during the discharge period, R looks like an open circuit. Therefore, the capacitor discharges with a time constant τ_2,

$$\tau_2 = R_N C = 10ms$$

targeting at a final value

$$V_{f2} = 0$$

When v(t) decreases to 10V ($I_N = 10mA$ through the bulb R_N=1k), the bulb opens up again. A new cycle starts.

Notice $\tau_2 << \tau_1$, so the flash rate is dominated by the charging time.

$$v(t) = 90 - (90 - 10)*e^{-T/\tau 1} = 65$$

$$T = 1.16\tau_1 = 11.6s$$

Therefore,

$$f = 1/T = 0.086 \text{ Hz}$$

4. *[20 Points]*: Agarwal and Lang, Problem 10.23

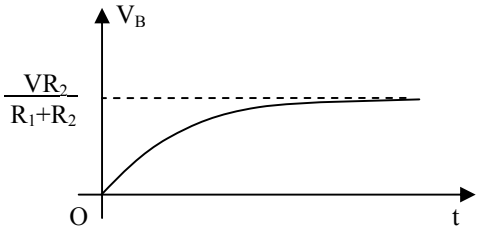
Answer:

(a) With finite R_2 and C_2,

$v_B(t=0^+) = 0$

$v_B(t=\infty) = VR_2/(R_1+R_2)$

$\tau_1 = (R_1||R_2)(C_1+C_2)$

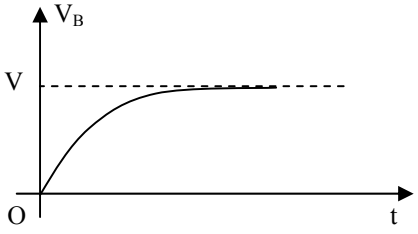


With $R_2 = \infty$ and $C_2 = 0$ (ideal probe),

$v_B(t=0^+) = 0$

$v_B(t=\infty) = V$

$\tau_2 = R_1C_1$



A non-ideal probe can introduce an error to the final value (measurement), and it may affect the shape of the waveform as well.

(b) i) Immediately after the step is applied, the circuit looks like a capacitor divider.

$v_B(t=0^+) = VC_3/(C_2+C_3)$

* Explanation (if you don't like the idea of capacitor dividers): at t = 0+, the capacitors look like short circuits (low impedance), so the capacitors dominate the resistors/capacitor parallel combination. Right at the point the step is applied, the amount of charge dumped onto both capacitors is the same, Q. Therefore,

$$Q/C_2 + Q/C_3 = V$$

So,

$$Q = VC_2C_3/(C_2+C_3)$$

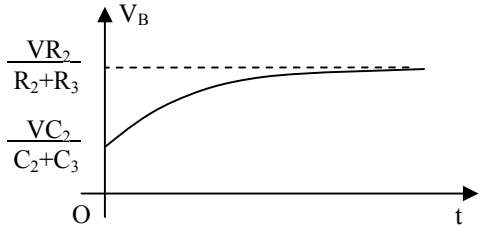
$$v_B(t=0^+) = Q/C_2 = VC_3/(C_2+C_3)$$

ii) As $t \rightarrow \infty$, the circuit looks like a resistor divider.

$v_B(t=\infty) = VR_2/(R_2+R_3)$

iii) $\tau_3 = (R_2||R_3)(C_2+C_3)$

$v_B(t)=VR_2/(R_2+R_3)+V[C_3/(C_2+C_3)-R_2/(R_2+R_3)]e^{-t/\tau 3}$ $(t > 0)$



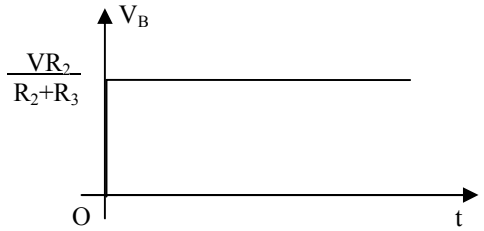
iv) If $C_3/(C_2+C_3) = R_2/(R_2+R_3)$,
that is,

$$R_2C_2 = R_3C_3$$

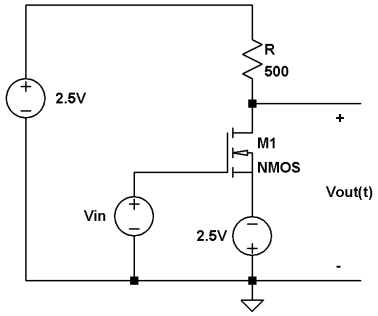
then the coefficient of the exponential term becomes zero,

$v_B(t) = VR_2/(R_2+R_3)$ $(t > 0)$

There will be no transient response.



5. *[20 Points]*: This problem makes use of the ELVIS iLab to study the small-signal characteristics of a common-source MOSFET-resistor amplifier. The amplifier is shown below. The transistor is the 2N7000 MOSFET that you have characterized in previous homework. Suitable parameters for this transistor are K = 0.14 A/V^2 and V_T = 1.9 V. The resistor has a nominal value of 500Ω. Notice that in this amplifier, the top power supply is set to +2.5V, and the bottom power supply is set to −2.5V, both with respect to ground. This is to allow an optimum bias point at the output that is right around 0 V with respect to ground. In this problem, you will measure the transfer characteristics of the amplifier and the small-signal voltage gain, and compare the voltage gain to a prediction based on the models developed in class.



(A) *[5 Points]* The transfer characteristics of this amplifier can be obtained by sweeping the input voltage between −2.5V and 2.5V. To do so, apply a sine wave at the input with a frequency of 100Hz, an amplitude of 2.5V and an offset of 0V. At the output, appropriately configure the oscilloscope to see at least one full period of the output signal with good resolution. To graph the transfer characteristics, graph v_{OUT} against v_{IN}. Print a screen shot of the canvas showing the transfer characteristics.

Using the Tracking feature in the bottom left corner of the client, read off the input bias voltage, VIN, that results in an output bias voltage, V_{OUT}, that is close to 0 V. Give these values.

(B) *[5 Points]* Now, measure the small-signal gain at the bias point that you just determined. To do so, reduce the input amplitude to 100mV, and apply the offset found in Part (A) such that the output is biased close to 0V. When you do this, you will see that the instrument is not

perfectly precise and that the input bias is a bit different from what you program. You will need to try different offset values until you get close enough. Once the output bias voltage is within about ±300mV of 0V, it is good enough. For this case, plot the waveforms of the input voltage and the output voltage versus time. Print a screen shot of this plot. Measure the amplitudes of both signals and determine the voltage gain.

(C) *[5 Points]* Next, obtain the input and output waveforms and extract the gain for other bias points. Bias the input 0.6V below (more negative than) the bias point you selected for Part (B). Plot the input and output waveforms, print a screen shot of this plot, measure the amplitudes of both signals, and extract the voltage gain. Do the same for an input bias 0.3V above (more positive than) the bias point you selected for Part (B). Plot and measure the same parameters. Comment on the change in voltage gain and the distortion that you observe in the output waveforms. Explain its origin in both cases.

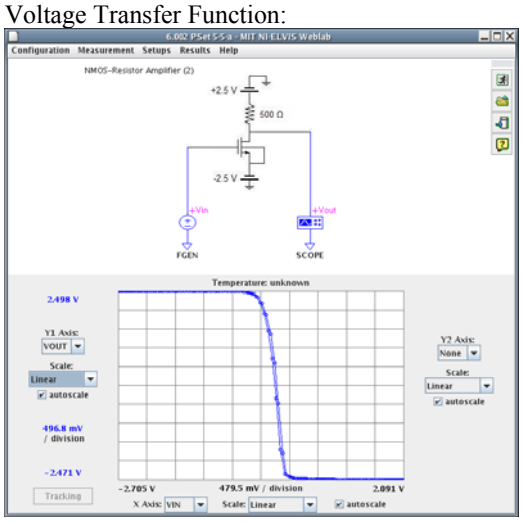
(D) *[5 Points]* Finally, use an appropriate small-signal model to calculate the voltage gain of this amplifier for an input bias such that the biased output voltage is equal to 0V. Use the parameters for the transistor given above. Compare what you obtain against the measurement results obtained in Part (B) above. Comment appropriately.

As always, start this problem early to avoid any last minute crunch on the system.

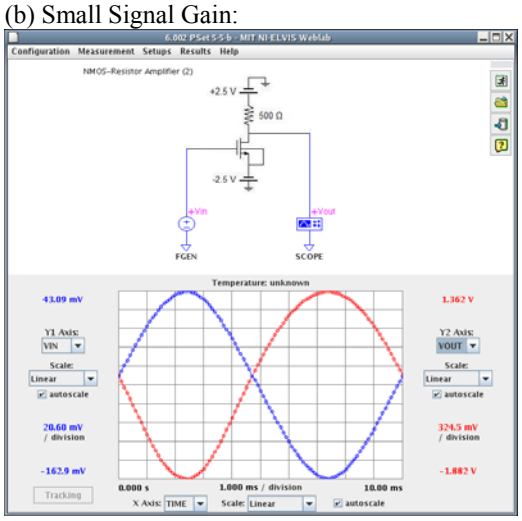
Answer:

(a) Reading from the graph below, when v_{IN} = 23mV, v_{OUT} is close to zero. (This may vary from run to run.)

Voltage Transfer Function:



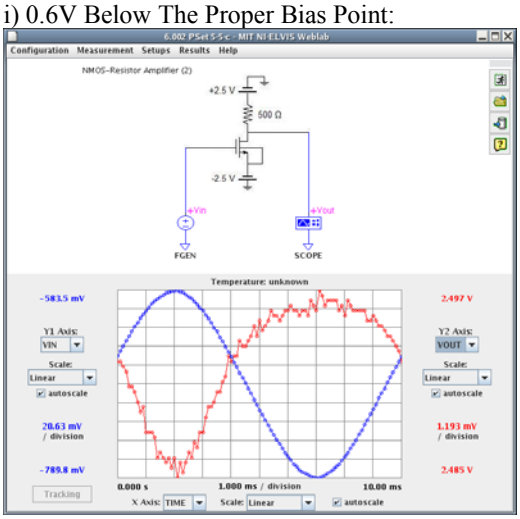
(b) Small Signal Gain:



$v_{IN,\,pp}$ = 43.09 – (–162.9) = 206 mV
$v_{OUT,\,pp}$ = 1.362 – (–1.882) = 3.24 V
$A_V = |v_{OUT,\,pp}/v_{IN,\,pp}| = 15.7$

(Note: It is ok if you think the gain is negative; and it is, or you can think there is a 180º phase shift.)

(c)
i) 0.6V Below The Proper Bias Point:



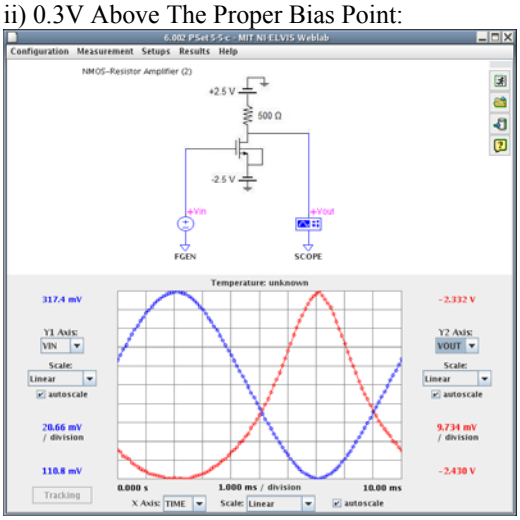
$v_{IN,\,pp}$ = –583.5 – (–789.8) = 206 mV
$v_{OUT,\,pp}$ = 2.497 – (2.485) = 12 mV
$A_V = |v_{OUT,\,pp}/v_{IN,\,pp}| = 0.058$

The voltage gain is much smaller than that in saturation, because the bias voltage,

2.5 – 0.6 = 1.9V

which is near V_T, the device is near cutoff. The distortion is large because the voltage transfer function is no longer linear in this case.

ii) 0.3V Above The Proper Bias Point:



$v_{IN,\,pp}$ = 317.4 – 110.8 = 206 mV
$v_{OUT,\,pp}$ = – 2.332 – (–2.430) = 98 mV
$A_V = |v_{OUT,\,pp}/v_{IN,\,pp}| = 0.48$

The voltage gain is also much smaller than that in saturation, because the bias voltage is too high, and the device is pushed into triode (linear) region. The distortion is large because the voltage transfer function is also non-linear in the triode region.

(d) $g_m = K(V_{GS} – V_T) = 0.14*(2.5 – 1.9) = 84$ mS
$A_V = g_m R = 84\text{mS} * 500 = 42$

This result is larger than the measurement. Here are a few possible reasons:

1) The K of the MOSFET is smaller than the theoretical value, 0.14A/V^2.

2) The actual V_{GS} is lower than 2.5V.

(There can be more acceptable reasons.)