HARDWARE REFERENCE MANUAL

PMAC2A-PC/104 CPU

PMAC2A-PC/104 CPU Hardware Reference

4xx-603670-xAxx

July 29, 2008

DELTA TAU
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REVISION HISTORY				
REV.	**DESCRIPTION**	**DATE**	**CHG**	**APPVD**
1	UPDATED JUMPER DESCRIPTIONS PGS. 6 & 30	05/17/06	CP	S. MILICI
2	REVS: J4, E20-23, CONNECTOR PINOUTS, & BOARD DIAGRAMS	10/04/06	CP	P. SHANTZ
3	CORRECTED TYPO IN I-VARIABLE SETTINGS, P. 17	01/22/08	CP	S.MILICI
4	CORRECTED USER FLAGS FOR PINS 25 & 26, P.36	07/29/08	CP	C.COKER

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INTRODUCTION

The PMAC2A PC/104 motion controller is a compact, cost-effective version of Delta Tau's PMAC2 family of controllers. The PMAC2A PC/104 can be composed of three boards in a stack configuration.

The CPU provides four channels of either DAC ±10V or pulse and direction command outputs. The optional axis expansion board provides a set of four additional servo channels and I/O ports. The optional communications board provides extra I/O ports and either the USB or Ethernet interface for faster communications.

Board Configuration

Base Version

The base version of the PMAC2A PC/104 ordered with no options provides a 90mm x 95mm board with:

- 40 MHz DSP563xx CPU (80 MHz 560xx equivalent)
- 128k x 24 internal zero-wait-state SRAM
- 512k x 8 flash memory for user backup and firmware
- Latest released firmware version
- RS-232 serial interface
- Four channels axis interface circuitry, each including:
  - 12-bit ±10V analog output
  - Pulse-and-direction digital outputs
  - 3-channel differential/single-ended encoder input
  - Four input flags, two output flags
  - Three PWM top-and-bottom pairs (unbuffered)
- 50-pin IDC header for amplifier/encoder interface
- 34-pin IDC header for flag interface
- PID/notch/feed forward servo algorithms
- 1-year warranty from date of shipment
- One CD-ROM per set of one to four PMACs in shipment (Cables, mounting plates, mating connectors not included)

PMAC2A-PC/104 Base Board shown

Board Options

Option 2A: PC/104 Bus Stack Interface

Option 2A provides the PC/104 bus interface allowing bus communications between a PC/104 type computer and the PMAC2A PC/104 motion controller.

Option 5xF: CPU Speed Options

- Option 5CF: 80 MHz DSP563xx CPU (160 MHz 56002 equivalent)
- Option 5EF: 160 MHz DSP563xx CPU (320 MHz 56002 equivalent)

Option 6: Extended Firmware Algorithm

Option 6 provides an Extended (Pole-Placement) Servo Algorithm firmware instead of the regular servo algorithm firmware. This is required only in difficult-to-control systems (resonances, backlash, friction, disturbances, changing dynamics).

Option 6L: Multi-block Lookahead Firmware

Option 6L provides a special lookahead firmware for sophisticated acceleration and cornering profiles execution. With the lookahead firmware PMAC controls the speed along the path automatically (but without changing the path) to ensure that axis limits are not violated.

Option 10: Firmware Version Specification

Normally the PMAC2A PC/104 is provided with the newest released firmware version. A label on the memory IC shows the firmware version loaded at the factory. Option 10 provides for a user-specified firmware version.

Option 12: Analog-to-Digital Converters

Option 12 permits the installation of two channels of on-board analog-to-digital converters with ±10V input range and 12-bits resolution. The key component installed with this option is U20.

Additional Accessories

Acc-1P: Axis Expansion Piggyback Board

Acc-1P provides four additional channels axis interface circuitry for a total of eight servo channels, each including:

- 12-bit ±10V analog output
- Pulse-and-direction digital outputs
- 3-channel differential/single-ended encoder input
- Four input flags, two output flags
- Three PWM top-and-bottom pairs (unbuffered)

Acc-1P Option 1: I/O Ports

Option 1 provides the following ports on the Acc-1P axes expansion board for digital I/O connections.

- Multiplexer Port: This connector provides eight input lines and eight output lines at TTL levels. When using the PMAC Acc-34x type boards these lines allow multiplexing large numbers of inputs and outputs on the port. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.
- I/O Port: This port provides eight general-purpose digital inputs and eight general-purpose digital outputs at 5 to 24Vdc levels. This 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules when different voltage levels or opto-isolation to the PMAC2A PC/104 is necessary.
- Handwheel port: this port provides two extra channels, each jumper selectable between encoder input or pulse output.

Acc-1P Option 2: Analog-to-Digital Converters

Option 2 permits the installation on the Acc-1P of two channels of analog-to-digital converters with ±10V input range and 12-bits resolution. The key component installed with this option is U20.

Acc-2P: Communications Board

Without any options, the PMAC2A PC/104 communicates through the RS-232 serial interface (using the optional Acc-3L flat cable) or PC/104 bus. This board provides added communication and I/O features.

Acc-2P Option 1A: USB Interface

Option 1A it provides a 480 Mbit/sec USB 2.0 interface.

Acc-2P Option 1B: Ethernet Interface

Option 1B provides a 100 Mbit/sec Ethernet.

Acc-2P Option 2: DPRAM Circuitry

Option 2 provides an 8K x 16 dual-ported RAM used with USB, Ethernet or PC/104 bus applications. If using for USB or Ethernet communications, Acc-2P-Opt-1A or Acc-2P-Opt-1B must be ordered. If used

for PC/104-bus communications, PMAC2A PC/104 Option-2A must be ordered. The key component installed with this option is U17. USB/Ethernet and PC/104 bus communications cannot be made simultaneously it is jumper selectable.

Acc-2P Option 3: I/O Ports

Option 3 provides the following ports on the Acc-2P communications board for digital I/O connections.

- Multiplexer Port: this connector provides eight input lines and eight output lines at TTL levels. When using the PMAC Acc-34x type boards these lines allow multiplexing large numbers of inputs and outputs on the port. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.
- I/O Port: this port provides 16 general-purpose digital I/O lines at TTL levels and these can be configured as all inputs, all outputs or eight inputs and eight outputs.
- Handwheel port: this port provides two extra channels, each jumper selectable between encoder input or pulse output.

Acc-8TS Connections Board

Acc-8TS is a stack interface board to for the connection of either one or two Acc-28B A/D converter boards. When a digital amplifier with current feedback is used, the analog inputs provided by the Acc-28B cannot be used.

Acc-8ES Four-Channel Dual-DAC Analog Stack Board

Acc-8ES provides four channels of 18-bit dual-DAC with four DB-9 connectors. This accessory is stacked to the PMAC2A PC/104 board and it is mostly used with amplifiers that require two ±10 V command signals for sinusoidal commutation.

Acc-8FS Four-Channel Direct PWM Stack Breakout Board

Acc-8FS it is a 4-channel direct PWM stack breakout board for PMAC2A PC/104. This is used for controlling digital amplifiers that require direct PWM control signals. When a digital amplifier with current feedback is used, the analog inputs provided by the Option 12 of the PMAC2A PC/104 (the Option 2 of the Acc-1P or the Acc-28B) could not be used.

HARDWARE SETUP

On the PMAC2 PC/104 CPU, there are a number of jumpers called E-points or W-points. That customize the hardware features of the CPU for a given application and must be setup appropriately. The following is an overview grouped in appropriate categories. For an itemized description of the jumper setup configuration, refer to the E-Point Descriptions section.

Clock Configuration Jumpers

E1: Servo and Phase Clock Direction Control – Jumper E1 should be OFF if the board is to use its own internally generated phase and servo clock signals. In this case, these signals are output on spare pins on the J8 RS-232 serial-port connector, where they can be used by other PMAC controllers set up to take external phase and servo clock signals.

Jumper E1 should be ON if the board is to use externally generated phase and servo clock signals brought in on the J8 RS-232 serial port connector. In this case, typically the clock signals are generated by another PMAC controller and output on its serial port connector.

If E1 is ON for external phase and clock signals, and these clock signals are not brought in on the serial port connector, the watchdog timer will trip almost immediately and shut down the board.

E2 and E4: CPU Frequency Control Jumpers – When the PMAC I46 I- variable is set to zero jumpers E2 and E4 on the base PMAC2A PC/104 board control the frequency at which the CPU will operate (or attempt to operate). Generally, this will be the highest frequency at which the CPU is rated to operate. Note that it is always possible to operate a CPU at a frequency lower than its maximum rating. While it may be possible to operate an individual processor at a frequency higher than its maximum rating, particularly at low ambient temperatures, performance cannot be guaranteed at such a setting, and this operation is done completely at the user's own risk.

- If jumpers E2 and E4 are both OFF, the CPU will operate at a 40 MHz frequency.
- If E2 is ON and E4 is OFF, the CPU will operate at a 60 MHz frequency.
- If E2 is OFF and E4 is ON, the CPU will operate at an 80 MHz frequency.

If I46 is set to a value greater than 0, the operational frequency is set to 10MHz * (I46 + 1), regardless of the jumper setting. See the Software Setup section for details on this.

E8: Phase Clock Lines Output Enable – Jump pin 1 to 2 to enable the Phase clock line on the J8 connector. Remove jumper to disconnect the Phase clock line on the J8 connector.

E9: Servo Clock Lines Output Enable – Jump pin 1 to 2 to enable the Servo clock line on the J8 connector. Remove jumper to disconnect the Servo clock line on the J8 connector.

Reset Jumpers

E0: Forced Reset Control – Remove E0 for normal operation. Installing E0 forces PMAC to a reset state, this configuration is for factory use only; the board will not operate with E0 installed.

E3: Re-Initialization on Reset Control – If E3 is OFF (default), PMAC executes a normal reset, loading active memory from the last saved configuration in non-volatile flash memory. If E3 is ON, PMAC re-initializes on reset, loading active memory with the factory default values.

E13: Firmware Load Jumper – If jumper E13 is ON during power-up/reset, the board comes up in bootstrap mode which permits loading of firmware into the flash-memory IC. When the PMAC Executive program tries to establish communications with a board in this mode, it will detect automatically that the board is in bootstrap mode and ask what file to download as the new firmware.

Jumper E13 must be OFF during power-up/reset for the board to come up in normal operational mode.

CPU Configuration Jumpers

E15A-E15C: Flash Memory Bank Select Jumpers – The flash-memory IC in location U10 on the PMAC2A PC/104 base board has the capacity for eight separate banks of firmware, only one of which can be used at any given time. The eight combinations of settings for jumpers E15A, E15B, and E15C select which bank of the flash memory is used. In the factory production process, firmware is loaded only into Bank 0, which is selected by having all of these jumpers OFF.

E10-E12: Power-Up State Jumpers – Jumper E10 must be OFF, jumper E11 must be ON, and jumper E12 must be ON, in order for the CPU to copy the firmware from flash memory into active RAM on power-up/reset. This is necessary for normal operation of the card. (Other settings are for factory use only.)

E14: Watchdog Timer Jumper – Jumper E14 must be OFF for the watchdog timer to operate. This is a very important safety feature, so it is vital that this jumper be OFF for normal operation. E14 should only be put ON to debug problems with the watchdog timer circuit.

W1: Flash chip select – Jumper W1 in position 1-2 selects a 28F320J3A part for the U10 flash chip. Jumper W1 in position 2-3 selects a 28F320J5A part for the U10 flash chip. This jumper is installed in the factory and must not be changed from its default state.

Communication Jumpers

E18-E19: PC/104 Bus Base Address Control – Jumpers E18 and E19 on the PMAC2A PC/104 CPU determine the base address of the card in the I/O space of the host PC. Together, they specify four consecutive addresses on the bus where the card can be found. The jumpers form the base address in the following fashion:

E18	E19	Address (hex)	Address (dec.)
OFF	OFF	$200	512
OFF	ON	$210	528
ON	OFF	$220	544
ON	ON	$230	560

The default base address is 528 ($210) formed with jumper E18 removed and E19 installed. This setting is necessary when using the USB or Ethernet ports of the Acc-2P communications board.

ADC Configuration Jumpers

E16: ADC Enable Jumper – Install E16 to enable the analog-to-digital converter circuitry ordered through Option-12. Remove this jumper to disable this option, which might be necessary to control motor 1 through a digital amplifier with current feedback.

Encoder Configuration Jumpers

E20-E23: Encoder Single Ended/Differential Select – PMAC has differential line receivers for each encoder channel, but can accept either single-ended (one signal line per channel) or differential (two signal lines, main and complementary, per channel). A jumper for each encoder permits customized configurations, as described below.

Single-Ended Encoders

With the jumper for an encoder set for single-ended, the differential input lines for that encoder are tied to 2.5V; the single signal line for each channel is then compared to this reference as it changes between 0 and 5V.

When using single-ended TTL-level digital encoders, the differential line input should be left open, not grounded or tied high; this is required for The PMAC differential line receivers to work properly.

Differential Encoders

Differential encoder signals can enhance noise immunity by providing common-mode noise rejection. Modern design standards virtually mandate their use for industrial systems, especially in the presence of PWM power amplifiers, which generate a great deal of electromagnetic interference.

Connect pin 1 to 2 to tie differential line to +2.5V

- Tie to +2.5V when no connection
- Tie to +2.5V for single-ended encoders

Connect pin 2 to 3 to tie differential line to +5V

- Don't care for differential line driver encoders
- Tie to +5V for complementary open-collector encoders (obsolete)

MACHINE CONNECTIONS

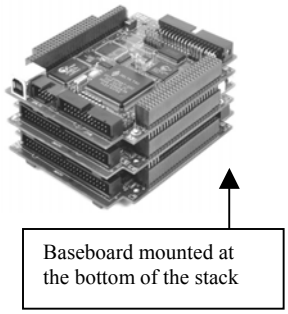
Typically, the user connections are made to terminal blocks that attach to the JMACH connectors by a flat cable. The following are the terminal blocks recommended for connections:

- 34-Pin IDC header to terminal block breakouts (Phoenix part number 2281063) Delta Tau part number 100-FLKM34-000
- 50-Pin IDC header to terminal block breakouts (Phoenix part number 2281089) Delta Tau part number 100-FLKM50-000

Mounting

The PMAC2A PC/104 is typically installed using standoffs when stacked to a PC/104 computer or as a stand-alone controller. At each of the four corners of the PMAC2A PC/104 board, there are mounting holes that can be used for this.

The PMAC2A PC/104 CPU is placed always at the bottom of the stack. The order of the Acc-1P or Acc-2P with respect to the CPU does not matter.



Power Supplies

Digital Power Supply

3A @ +5V (±5%) (15 W) with a minimum 5 msec rise time

(Eight-channel configuration, with a typical load of encoders)

The PMAC2A PC/104, the Acc-1P and the Acc-2P each require a 1A @ 5VDC power supply for operation. Therefore, a 3A @ 5VDC power supply is recommended for a PMAC2A PC/104 board stack with Acc-1P and Acc-2P boards.

- The host computer provides the 5 Volts power when installed in the PC/104 bus and cannot be disconnected. In this case, there must be no external +5V supply, or the two supplies will "fight" each other, possibly causing damage. This voltage could be measured on the TB1 terminal block or the JMACH1 connector.
- In a stand-alone configuration, when PMAC is not plugged in a computer bus, it will need an external 5V supply to power its digital circuits. The 5V power supply can be brought in either from the TB1 terminal block or from the JMACH1 connector.
- When an ACC-2P is used, a minimum rise time of 5 msec is a requirement of the power supply. In addition, the power supply ramp-down time should not exceed 20 msec. While solutions to this issue can involve complex circuitry that minimizes power loss during normal operation, the simplest method of quickly bringing down the power rail is to add a bleed-down resistor between VCC and GND. The resistor should be large enough that it does not cause unnecessary power consumption, while still discharging the bulk capacitance as quickly as possible. Specific resistor values will depend on the overall design of the system, but in general the voltage drop-off time should not exceed 20 msec. A value that has been found to work for some systems is 18k.

DAC Outputs Power Supply

0.3A @ +12 to +15V (4.5W)
0.25A @ -12 to -15V (3.8W)
(Eight-channel configuration)

- The host computer provides the ±12 Volts power supply in the case PMAC is installed in the PC/104 bus. With the board stack into the bus, it will pull ±12V power from the bus automatically and it cannot be disconnected. In this case, there must be no external ±12V

supply, or the two supplies will fight each other, possibly causing damage. This voltage could be measured on the TB1 terminal block.

- In a stand-alone configuration, when PMAC is not plugged in a computer bus, it will need an external ±12V supply only when the digital-to-analog converter (DAC) outputs are used. The ±12V lines from the supply, including the ground reference, can be brought in either from the TB1 terminal block or from the JMACH1 connector.

Flags Power Supply

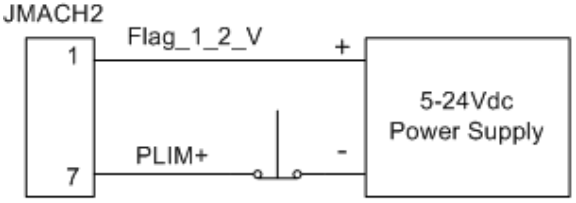
Each channel of PMAC has five dedicated digital inputs on the machine connector: PLIMn, MLIMn (overtravel limits), HOMEn (home flag), FAULTn (amplifier fault), and USERn. A power supply from 5 to 24V must be used to power the circuits related to these inputs. This power supply can be the same used to power PMAC and can be connected from the TB1 terminal block or the JMACH1 connector.

Overtravel Limits and Home Switches

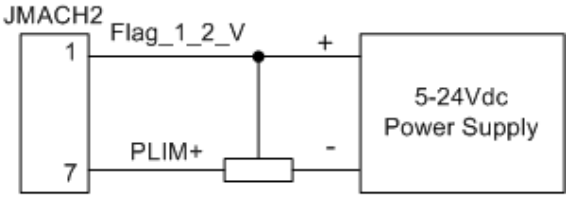
When assigned for the dedicated uses, these signals provide important safety and accuracy functions. PLIMn and MLIMn are direction-sensitive over-travel limits that must conduct current to permit motion in that direction. If no over-travel switches will be connected to a particular motor, this feature must be disabled in the software setup through the PMAC Ix25 variable.

Types of Overtravel Limits

PMAC expects a closed-to-ground connection for the limits to not be considered on fault. This arrangement provides a failsafe condition. Usually, a passive normally close switch is used. If a proximity switch is needed instead, use a 5 to 24V normally closed to ground NPN sinking type sensor.



Dry Contact



15-24V proximity

Home Switches

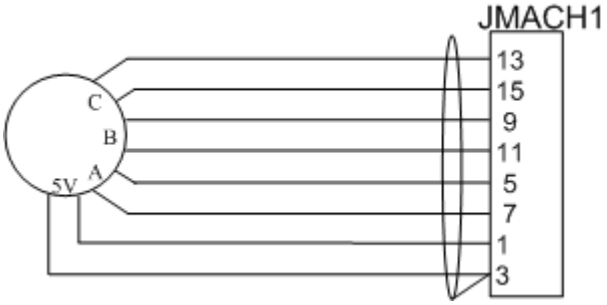
While normally closed-to-ground switches are required for the overtravel limits inputs, the home switches could be either normally close or normally open types. The polarity is determined by the home sequence setup, through the I-variables I9n2.

Motor Signals Connections

Incremental Encoder Connection

Each JMACH1 connector provides two +5V outputs and two logic grounds for powering encoders and other devices. The +5V outputs are on pins 1 and 2; the grounds are on pins 3 and 4. The encoder signal pins are grouped by number: all those numbered 1 (CHA1+, CHA1-, CHB1+, CHC1+, etc.) belong to encoder #1. The encoder number does not have to match the motor number, but usually does. Connect the A and B (quadrature) encoder channels to the appropriate terminal block pins. For encoder 1, the CHA1+ is pin 5 and CHB1+ is pin 9. If there is a single-ended signal, leave the complementary signal pins floating – do not ground them. However, if single-ended encoders are used, check the setting of the resistor packs (see the Hardware Setup section for details). For a differential encoder, connect the complementary signal lines – CHA1- is pin 7, and CHB1- is pin 11. The third channel (index pulse) is optional; for encoder 1, CHC1+ is pin 13, and CHC1- is pin 15.

Example: differential quadrature encoder connected to channel #1:



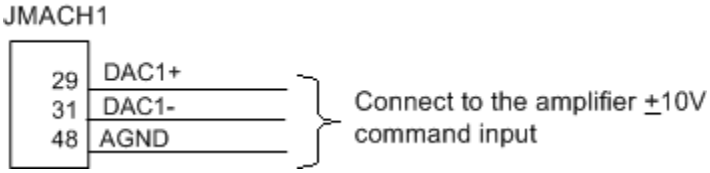
DAC Output Signals

If PMAC is not performing the commutation for the motor, only one analog output channel is required to command the motor. This output channel can be either single-ended or differential, depending on what the amplifier is expecting. For a single-ended command using PMAC channel 1, connect DAC1+ (pin 29) to the command input on the amplifier. Connect the amplifier's command signal return line to PMAC's GND line (pin 48). In this setup, leave the DAC1- pin floating; do not ground it.

For a differential command using PMAC channel 1, connect DAC1 (pin 29) to the plus-command input on the amplifier. Connect DAC1- (pin 31) to the minus-command input on the amplifier. PMAC's GND should still be connected to the amplifier common.

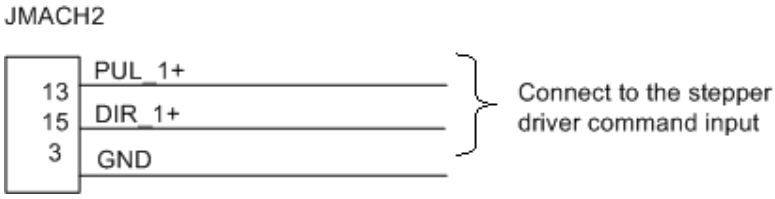
Any analog output not used for dedicated servo purposes may be utilized as a general-purpose analog output by defining an M-variable to the command register, then writing values to the M-variable. The analog outputs are intended to drive high-impedance inputs with no significant current draw. The 220Ω output resistors will keep the current draw lower than 50 mA in all cases and prevent damage to the output circuitry, but any current draw above 10 mA can result in noticeable signal distortion.

Example:



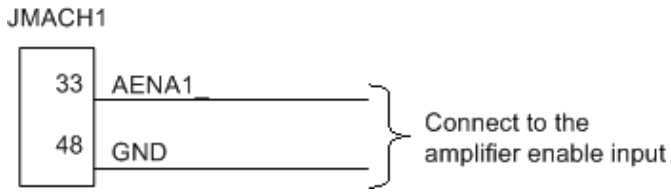
Pulse and Direction (Stepper) Drivers

The channels provided by the PMAC2A PC/104 board or the Acc-1P board can output pulse and direction signals for controlling stepper drivers or hybrid amplifiers. These signals are at TTL levels.



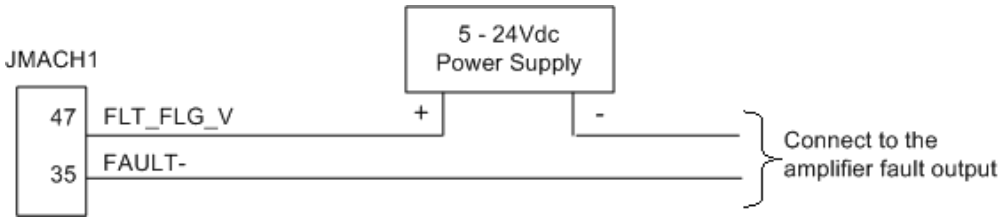
Amplifier Enable Signal (AENAx/DIRn)

Most amplifiers have an enable/disable input that permits complete shutdown of the amplifier regardless of the voltage of the command signal. PMAC's AENA line is meant for this purpose. AENA1- is pin 33. This signal is an open-collector output and an external 3.3 kΩ pull-up resistor can be used if necessary.



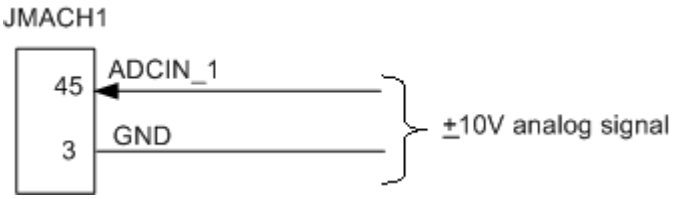
Amplifier Fault Signal (FAULT-)

This input can take a signal from the amplifier so PMAC knows when the amplifier is having problems, and can shut down action. The polarity is programmable with I-variable Ix25 (I125 for motor 1) and the return signal is ground (GND). FAULT1- is pin 35. With the default setup, this signal must actively be pulled low for a fault condition. In this setup, if nothing is wired into this input, PMAC will consider the motor not to be in a fault condition.



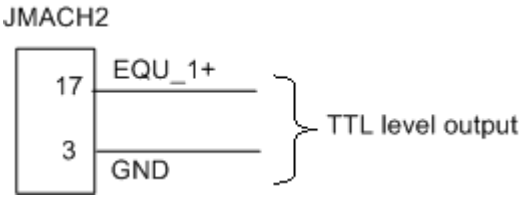
Optional Analog Inputs

The optional analog-to-digital converter inputs are ordered either through Option-12 on the CPU or Option-2 on the axes expansion board. Each option provides two 12-bit analog inputs analog inputs with a ±10Vdc range.



Compare Equal Outputs

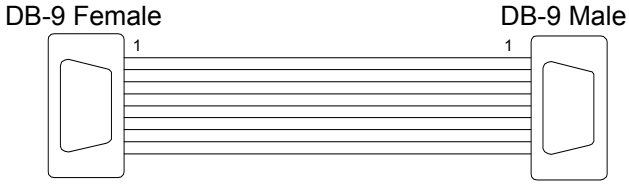
The compare-equals (EQU) outputs have a dedicated use of providing a signal edge when an encoder position reaches a pre-loaded value. This is very useful for scanning and measurement applications. Instructions for use of these outputs are covered in detail in the PMAC2 User Manual.



Serial Port (JRS232 Port)

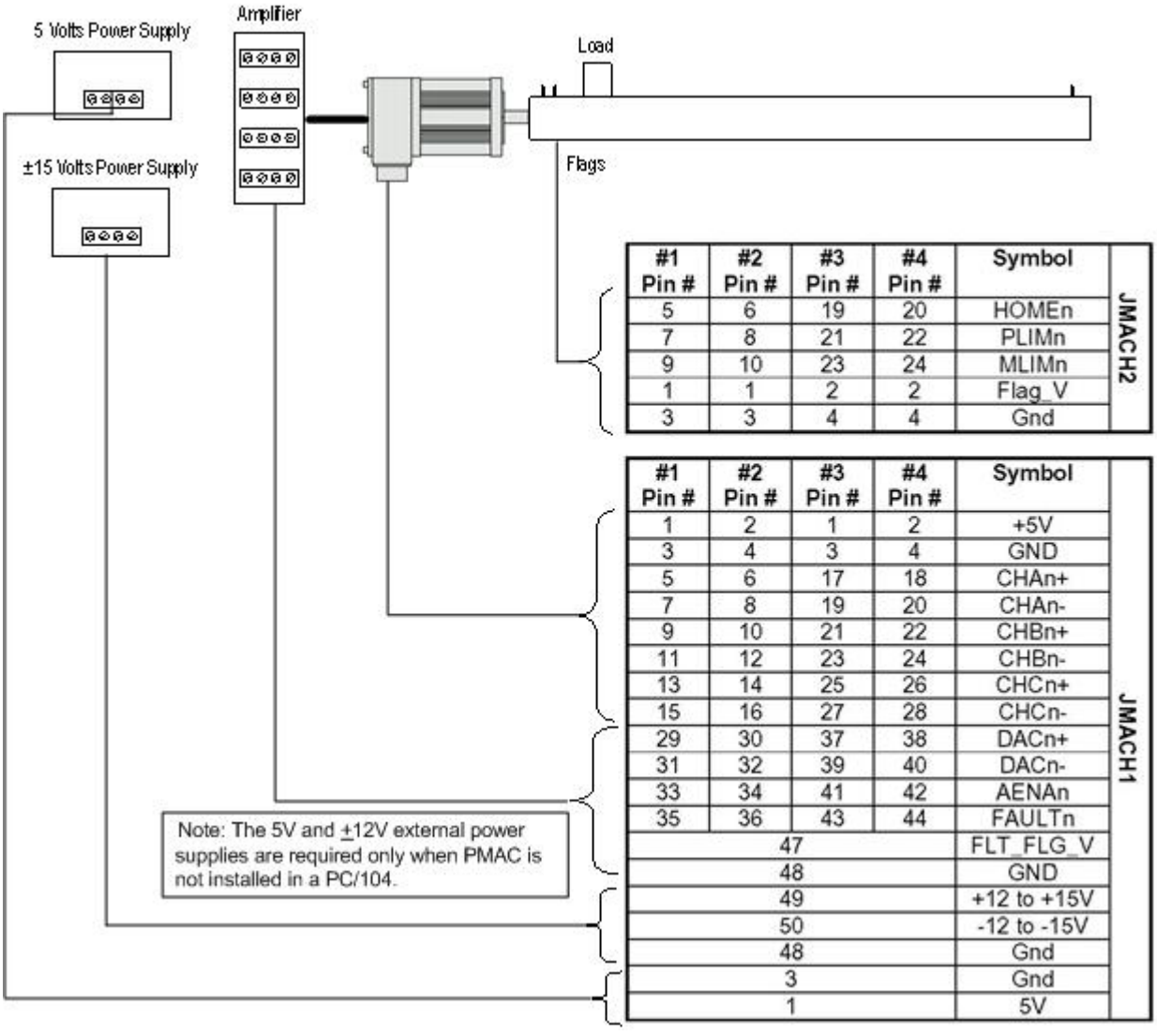
For serial communications, use a serial cable to connect your PC's COM port to the J8 serial port connector present on the PMAC2A PC/104 CPU. Delta Tau provides the Acc-3L cable for this purpose that connects the PMAC to a DB-9 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for your particular setup.

If a cable needs to be made, the easiest approach is to use a flat cable prepared with flat-cable type connectors as indicated in the following diagram:



PMAC (DB-9S)	PC (DB-9)
1 (No connect)	1 (No connect)
2 (TXD/)	2 (RXD)
3 (RXD/)	3 (TXD)
4 (DSR)	4 (DTR)
5 (Gnd)	5 (Gnd)
6 (DTR)	6 (DSR)
7 (CTS)	7 (RTS)
8 (RTS)	8 (CTS)
9 (No connect)	9 (No connect)

Machine Connections Example: Using Analog ±10V Amplifier



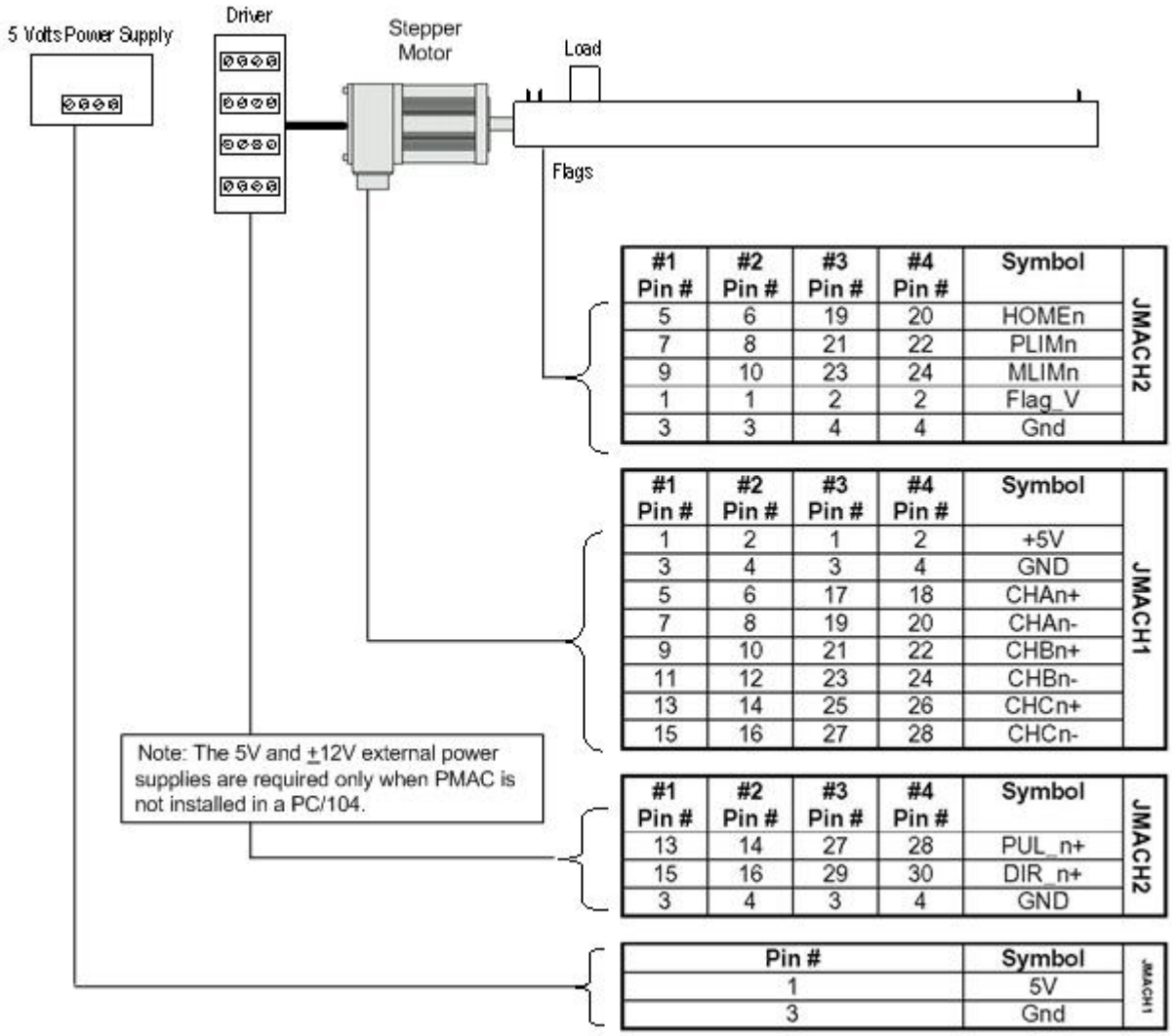
JMACH2

#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	Symbol
5	6	19	20	HOMEn
7	8	21	22	PLIMn
9	10	23	24	MLIMn
1	1	2	2	Flag_V
3	3	4	4	Gnd

JMACH1

#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	Symbol
1	2	1	2	+5V
3	4	3	4	GND
5	6	17	18	CHAn+
7	8	19	20	CHAn-
9	10	21	22	CHBn+
11	12	23	24	CHBn-
13	14	25	26	CHCn+
15	16	27	28	CHCn-
29	30	37	38	DACn+
31	32	39	40	DACn-
33	34	41	42	AENAn
35	36	43	44	FAULTn
47				FLT_FLG_V
48				GND
49				+12 to +15V
50				-12 to -15V
48				Gnd
3				Gnd
1				5V

Machine Connections Example: Using Pulse and Direction Drivers



#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	Symbol	
5	6	19	20	HOMEn	JMACH2
7	8	21	22	PLIMn	
9	10	23	24	MLIMn	
1	1	2	2	Flag_V	
3	3	4	4	Gnd	

#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	Symbol	
1	2	1	2	+5V	JMACH1
3	4	3	4	GND	
5	6	17	18	CHAn+	
7	8	19	20	CHAn-	
9	10	21	22	CHBn+	
11	12	23	24	CHBn-	
13	14	25	26	CHCn+	
15	16	27	28	CHCn-	

#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	Symbol	
13	14	27	28	PUL_n+	JMACH2
15	16	29	30	DIR_n+	
3	4	3	4	GND	

Pin #	Symbol	
1	5V	JMACH1
3	Gnd	

SOFTWARE SETUP

Note:

The PMAC2A PC/104 requires the use of V1.17 or newer firmware. There are few differences between the previous V1.16H firmware and the V1.17 firmware other than the addition of internal support for the Flex CPU design.

PMAC I-Variables

PMAC has a large set of Initialization parameters (I-variables) that determine the "personality" of the card for a specific application. Many of these are used to configure a motor properly. Once set up, these variables may be stored in non-volatile EAROM memory (using the **SAVE** command) so the card is always configured properly (PMAC loads the EAROM I-variable values into RAM on power-up).

The programming features and configuration variables for the PMAC2A PC/104 are described fully in the PMAC2 User and Software manuals.

Communications

Delta Tau provides software tools that allow communicating with of the PMAC2A PC/104 board by either its standard RS-232 port or the optional USB or Ethernet ports. PEWIN is the most important in the series of software accessories, and it allows configuring and programming the PMAC for any particular application.

Operational Frequency and Baud Rate Setup

Note:

Older PMAC boards required a start-up PLC for setting the operational frequency at 80 MHz. That method is not compatible with the PMAC2A PC/104 board and will shutdown the board when used.

The operational frequency of the CPU can be set in software by the variable I46. If this variable is set to 0, PMAC firmware looks at the jumpers E2 and E4 to set the operational frequency for 40, 60, and 80 MHz operation. If I46 is set to a value greater than 0, the operational frequency is set to 10MHz * (I46 + 1), regardless of the jumper setting. If the desired operational frequency is higher than the maximum rated frequency for that CPU, the operational frequency will be reduced to the rated maximum. It is always possible to operate the Flex CPU board at a frequency below its rated maximum. I46 is used only at power-up/reset, so to change the operational frequency, set a new value of I46, issue a **SAVE** command to store this value in non-volatile flash memory, then issue a **$$$** command to reset the controller.

To determine the frequency at which the CPU is actually operating, issue the **TYPE** command to the PMAC. The PMAC will respond with five data items, the last of which is `CLK Xn`, where *n* is the multiplication factor from the 20 MHz crystal frequency (not 10 MHz). *n* should be equivalent to (I46+1)/2 if I46 is not requesting a frequency greater than the maximum rated for that CPU board. *n* will be 2 for 40 MHz operation, 4 for 80 MHz operation, and 8 for 160 MHz operation.

If the CPU's operational frequency has been determined by (a non-zero setting of) I46, the serial communications baud rate is determined at power-up/reset by variable I54 alone according to the following table:

I54	Baud Rate	I54	Baud Rate
0	600	8	9600
1	900	9	14,400
2	1200	10	19,200
3	1800	11	28,800
4	2400	12	38,400
5	3600	13	57,600
6	4800	14	76,800
7	7200	15	115,200

For a saved value of 0 for I46, the serial baud rate is determined by the combination of I54 and the CPU frequency as shown in the following table.

I54	Baud Rate for 40 MHz CPU	Baud Rate for 60 MHz CPU	Baud Rate for 80 MHz CPU
0	600	Disabled	1200
1	900* (-0.05%)	900	1800* (-0.1%)
2	1200	1200	2400
3	1800* (-0.1%)	1800	3600* (-0.19%)
4	2400	2400	4800
5	3600* (-0.19%)	3600	7200* (-0.38%)
6	4800	4800	9600
7	7200* (-0.38%)	7200	14,400*(-0.75%)
8	9600	9600	19,200
9	14,400*(-0.75%)	14,400	28,800*(-1.5%)
10	19,200	19,200	38,400
11	28,800*(-1.5%)	28,800	57,600*(-3.0%)
12	38,400	38,400	76,800
13	57,600*(-3.0%)	57,600	115,200*(-6.0%)
14	76,800	76,800	153,600
15	Disabled	115,200	Disabled
* Not an exact baud rate			

Filtered DAC Output Configuration

The PMAC2 PC104 is a PMAC2 style board with default +/-10V outputs produced by filtering a PWM signal. This technique has been used been for some time now by many of our competitors. Although this technique does not contain the same levels of performance as a true Digital to Analog converter, for most servo applications it is more than adequate. Many of our customers using this product have migrated over from the PMAC1 style board with a true 16-bit DAC. This document is meant for explaining the tradeoffs of PWM frequency vs. resolution in the PMAC2PC104 base configuration as well as a comparison to the PMAC1 style 16 bit DACs.

Both the resolution and the frequency of the Filtered PWM outputs are configured in software on the PMAC2PC104 through the variable **I900**. This I900 variable also effects the phase and servo interrupts. Therefore as we change I900 we will also have to change **I901** (phase clock divider), **I902** (servo clock divider), and **I10** (servo interrupt time). These four variables are all related and must be understood before adjusting parameters.

Since the PMAC2PC104 uses standard PMAC2 firmware the following I-variables must be set properly to use the digital-to-analog (filtered DAC) outputs:

```
I900  = 1001              ; PWM frequency 29.4kHz, PWM 1-4
I901  = 5                 ; Phase Clock 9.8059kHz
I902  = 3                 ; Servo frequency 2.451kHz
I903  = 1746              ; ADC frequency
I906  = 1001              ; PWM frequency 29.4kHz, PWM 5-8
I907  = 1746              ; ADC frequency
I9n6  = 0                 ; Output mode: PWM
Ix69  = 1001              ; DAC limit 10Vdc
I10   = 3421867           ; Servo interrupt time
```

n = channel number from 1 to 8
x = motor number from 1 to 8

Parameters to Set up Global Hardware Signals

I900

I900 determines the frequency of the **MaxPhase** clock signal from which the actual phase clock signal is derived. It also determines the PWM cycle frequency for Channels 1 to 4. This variable is set according to the equation:

```
I900 = INT[117,964.8/(4*PWMFreq(KHz)) - 1]
```

The PMAC2 PC/104 filtered PWM circuits were optimized for 30KHz. **I900** should be set to 1088 (calculated as 27.06856KHz)

I901

I901 determines how the actual phase clock is generated from the **MaxPhase** clock, using the equation:

```
PhaseFreq(kHz) = MaxPhaseFreq(kHz)/(I901+1)
```

I901 is an integer value with a range of 0 to 15, permitting a division range of 1 to 16. Typically, the phase clock frequency is in the range of 8 kHz to 12 kHz. 9KHz is standard, set **I901** = 5 (calculated as 9.02285 KHz).

I902

I902 determines how the servo clock is generated from the phase clock, using the equation:

```
ServoFreq(KHz) = PhaseFreq(KHz)/(I902+1)
```

I902 is an integer value with a range of 0 to 15, permitting a division range of 1 to 16. On the servo update, which occurs once per servo clock cycle, PMAC2 updates commanded position (interpolates) and closes the position/velocity servo loop for all active motors, whether or not commutation and/or a digital current loop is closed by PMAC2. Typical servo clock frequencies are 1 to 4 kHz. The PMAC standard is 2.26 KHz, set **I902** = 3 (calculated as 2.25571 KHz).

I10 tells the PMAC2 interpolation routines how much time there is between servo clock cycles. It must be changed any time **I900**, **I901**, or **I902** is changed. **I10** can be set according to the formula:

```
I10 = (2*I900+3)(I901+1)(I902+1)*640/9
```

I10 should be set to 3718827.

I903

I903 determines the frequency of four hardware clock signals used for machine interface channels 1-4; This can be left at the default value (I903=*). The four hardware clock signals are SCLK (encoder sample clock), PFM_CLK (pulse frequency modulator clock), DAC_CLK (digital-to-analog converter clock), and ADC_CLK (analog-to-digital converter clock).

Parameters to Set Up Per-Channel Hardware Signals

I9n6

I9n6 is the output mode; "n" is the output channel number (i.e. for channel 1 the variable to set would be i916, i926 for channel 2 etc.). On Pmac1 there is only one output and one output mode, DAC output. On PMAC2 boards, each channel has 3 outputs, and there are 4 output modes. Since this is board was designed to output filtered PWM signals we want to configure at least the first output as PWM. Therefore the default value of 0 is the choice. For information on this variable consult the PMAC1/PMAC2 software reference manual.

Ix69

Ix69 is the motor output command limit. The analog outputs on PMAC1 style boards and some PMAC2 accessories are 16-bit DACs, which map a numerical range of -32,768 to +32,767 into a voltage range of -10V to +10V relative to analog ground (AGND). For our purposes of a filtered PWM output this value still represents the maximum voltage output; however the ratio is slightly different. With a true DAC, Ix69=32767 allows a maximum voltage of 10V output. With the filtered PWM circuit, Ix69 is a function of I900. A 10V signal in the output register is no longer 32767 as was in PMAC1, a 10V signal is corresponds to a value equal to I900. Anything over I900 will just rail the Dac at 10V. For Example:

Desired Maximum Output Value = 6V

```
Ix69=6/10 * i900
```

Desired Maximum Output Value = 10V

```
Ix69= I900 + 10; add a little headroom to assure a full 10V
```

Effects of Changing I900 on the System

It should now be understood that a full 10 volts is output when the output register is equal to i900. The output register is suggested m-variable Mx02 (I.e. M102-> Y:$C002,8,16,S ; OUT1A command value; DAC or PWM). With default setting of I900, 10Volts is output when m102 is equal to i900, or 1001. Since the output register is an integer value the smallest increment of change is about 10mV (1/1001 * 10V). Some users may want to calibrate their analog output using Ix29. Ix29 is an integer similar to Mx02 except the value is added to the output register every servo cycle to apply a digital offset to the output register. Therefore the resolution of our output signal affects how Ix29 should be set. As mentioned earlier, with the default parameters, 1 bit change in the output register changes the analog output by about 10mV. Therefore if there is an analog output offset less than 5mV, Ix29 cannot decrease your offset. By increasing I900 you increase your resolution, so if you double i900, 1 bit change in the output register corresponds to about 5mV. So with Ix29 you can only change the offset in increments of 5mV.

You can see above that by increasing I900 you increase the resolution of our command output register. This sounds like a good thing, right? There are tradeoffs when you change I900 between resolution and ripple.

By increasing I900 we are essentially decreasing our PWM Frequency. The two are related by the following equation:

```
I900 = INT[117,964.8/(4*PWMFreq(KHz)) - 1]
```

Passing the PWM signal through a 10KHz low pass filter creates the +/-10V signal output. The duty cycle of the PWM signal is what generates the magnitude the voltage output. The frequency of the PWM signal determines the magnitude and frequency of ripple on that +/-10V signal. As you lower the PWM frequency and subsequently increase your output resolution, you increase the magnitude of the ripple as well as slow down the frequency of the ripple as well. Depending on the system, this ripple can affect performance at different levels.

So what do we mean by ripple? Ripple is the small signal that will you will see on top of the +/-10V signal if you put an oscilloscope on it. In other words if I command a 4V signal out of the PMAC2PC104 and scope it, I will see a small sinusoidal type wave centered on 4V. At the default PWM frequency and output resolution this will have a magnitude of about 230mV and a frequency of about 33kHz. This is typically faster than any of the control loops so the amplifier essentially filters it out of the system.

Say I wanted to double the resolution of my output signal, I would merely double my I900 value from 1001 to 2002. How does this affect the ripple? From a test I calculated the ripple magnitude to increase from around 230mV to about 700mV. The frequency of the ripple decreased from about @30kHz to @15kHz. Here are some measurements taken with a PMAC2PC104:

I900 Value	**Output Resolution Signed**	**Voltage Output Change Per 1bit increment In output register**	**PWM Frequency**	**Approximate Ripple Magnitude**	**Approximate Ripple Frequency**
1001	@11 bit	9.9mV	29.4177 KHz	230mV	30KHz
2002	@12 bit	4.99mV	14.72 Khz	700mV	15KHz
4004	@13bit	2.49mV	7.36 Khz	2V	7Khz

How does the ripple affect servo performance? It really depends on the system. For most servo systems the mechanics can't respond anywhere near these frequencies. Some systems with linear amplifiers it will effect the performance especially as you lower the PWM frequency and effectively the ripple frequency, i.e. galvanometers, etc. In the overall majority of the servo world, these ripple frequencies will not show in the system due to mechanical and electrical time constants of most systems. This will happen regardless of the amplifier used.

So why is the recommended setup for 30KHz? A few reasons, the first is aesthetics. Nobody wants to put a scope on an output signal and see 1 or 2V of hash. If you increase that frequency the hash is minimized. The second reason is response of the output with respect to the servo filter. If you increase the output resolution and thus lower the PWM frequency far enough you will notice some lag in the system from the delays between the output register value actually being picked up by the slower PWM frequency.

For high response systems we suggest using Acc8es and a true 18bit DAC. However the filtered PWM technique will be more than adequate for most applications.

How does changing I900 effect other settings in PMAC

I900 is does not only set the PWM frequency for the PWM outputs but it also sets the Max Phase Frequency.

*MaxPhase Frequency = 117,964.8 kHz / [2*I900+3]*

*PWM Frequency = 117,964.8 kHz / [4*I900+6]*

The Max Phase Frequency is then divided by I901 to generate the frequency for the phase interrupt and its routines. **If you change I900 you have to change I901 to keep the same phase interrupt.**

PHASE Clock Frequency = MaxPhase Frequency / (I901+1)

The Phase Clock Frequency setting also effects the servo interrupt frequency. **If you change the phase interrupt frequency then you must change I902 to keep the same servo interrupt.**

Servo Clock Frequency = PHASE Clock Frequency / (I902+1)

When you change the servo interrupt you must always change the servo interrupt time, i10, to match or all of your timing will be off in PMAC.

*I10=8388608/(Servo Frequency (KHz)) = 8388608 * ServoTime(msec)*

If you decide to change I900 be sure to reset Ix69 to the proper safety setting per the following formula:

*Ix69=MaxVolts/10 * I900*

Examples:

Default Example:

```
I900=1001
I901=2
I902=3
Ix69=1024
I10=1710933
```

*MaxPhase Frequency = 117,964.8 kHz / [2*1001+3] = 58.835KHz*

*PWM Frequency = 117,964.8 kHz / [4*1001+6] = 29.418KHz*

PHASE Clock Frequency = MaxPhase Frequency / (2+1) = 19.61KHz

Servo Clock Frequency = PHASE Clock Frequency / (3+1) = 4.90KHz

I10=8388608/(4.902943) = 1710933

*Ix69=10V/10 * I900 = 1001 add headroom to 1024*

Now lets say I wanted to double my resolution:

I900=2002

*MaxPhase Frequency = 117,964.8 kHz / [2*2002+3] = 29.44KHz*

*PWM Frequency = 117,964.8 kHz / [4*2002+6] = 14.72KHz*

In order to save headroom on firmware routines that trigger off the phase and servo interrupts it is best to keep those frequencies about the same as above. Some systems may want higher phase and servo

interrupt frequencies for better servo performance, but our default frequencies are typically more than fast enough for many applications. We will discuss tuning parameter a bit later in this document.

I901= 29.44KHz/19.61KHz -1 = @0.5 set it at 1 or 14.72KHz

This is not exactly the same since I901 is an integer value but pretty close. Since we are doing any commutation with a +/-10V signal it doesn't make that much of a difference. The Servo Frequency we will be able to get close though:

I902=14.72KHz/4.9 – 1 = 2.004 or 2 which is @4.9KHz

For a 10V max signal output:

Ix69=i900 + headroom = 2024

We must set I10 whenever we change the servo clock but since we kept it basically the same, I19 stays pretty much the same. Without rounding it works out to the following:

```
I10 = 8388608/4.906613 = 1709653
```

For precise timing within your motion application it is important not to round off when calculating I10.

Effects of Output Resolution and Servo Interrupt Frequency on Servo Gains

When you change your output resolution and/or servo interrupt timing your tuning parameters will no longer respond the same. The system will have to be tuned again in order to achieve the desired performance. There is an approximate relation of output resolution to servo loop gains . If you were switching an application from a PMAC style 16bit Dac to a PMAC2Pc104 with default resolution of about 11bits you can expect a change of your gains in order to get similar response.

The max output value of the output command with a 16bit Dac is 32767. With the PMAC2Pc104 at its default parameters the max output value is 1001. If you had equal servo interrupt frequencies the proportional gain on the PC104 system would have a proportional gain 1001/32767 or about 1/32 smaller. This is more a rule of thumb than an exact formula. It is always recommended to go through a full tuning procedure when changing output resolution.

If you decide to change the Servo Interrupt Frequency, then you are also changing the dynamics of the servo filter and thus the system. You will need to retune the system in order to get the desired performance. If you increase the servo frequency you will need to lower the proportional gain in order to achieve similar performance. The reason you increased the frequency in the first place was more likely to achieve a higher performance so relations here are not very helpful.

If you desire to change servo interrupt frequency in order to have your foreground PLCs execute more often you can also adjust Ix60 to keep your gains the same, see the Pmac1/2 Software Reference Manual for a further description of this parameter.

Using Flag I/O as General-Purpose I/O

Either the user flags or other not assigned axes flag on the base board can be used as general-purpose I/O for up to 20 inputs and 4 outputs at 5-24Vdc levels. The indicated suggested M-variables definitions, which are defined in the PMAC2 Software reference, allows accessing each particular line according to the following table:

Flag	Type	Channel Number			
		#1	#2	#3	#4
HOME	5-24 VDC Input	M120	M220	M320	M420
PLIM	5-24 VDC Input	M121	M221	M321	M421
MLIM	5-24 VDC Input	M122	M222	M322	M422
USER	5-24 VDC Input	M115	M215	M315	M415
AENA	5-24 VDC Output	M114	M214	M314	M414

Note:

When using these lines as regular I/O points the appropriate setting of the Ix25 variable must be used to enable or disable the safety flags feature.

Analog Inputs Setup

The optional analog-to-digital converter inputs are ordered either through Option-12 on the CPU or Option-2 on the axes expansion board. Each option provides two 12-bit analog inputs with a ±10Vdc range. The M-variables associated with these inputs provided a range of values between +2048 and –2048 for the respective ±10Vdc input range. The following is the software procedure to setup and read these ports.

CPU Analog Inputs

```
I903 = 1746                ;Set ADC clock frequency at 4.9152 MHz
WX:$C014, $1FFFFF          ;Clock strobe set for bipolar inputs
M105->X:$0710,12,12,S      ;ADCIN_1 on JMACH1 connector pin 45
M205->X:$0711,12,12,S      ;ADCIN_2 on JMACH1 connector pin 46
```

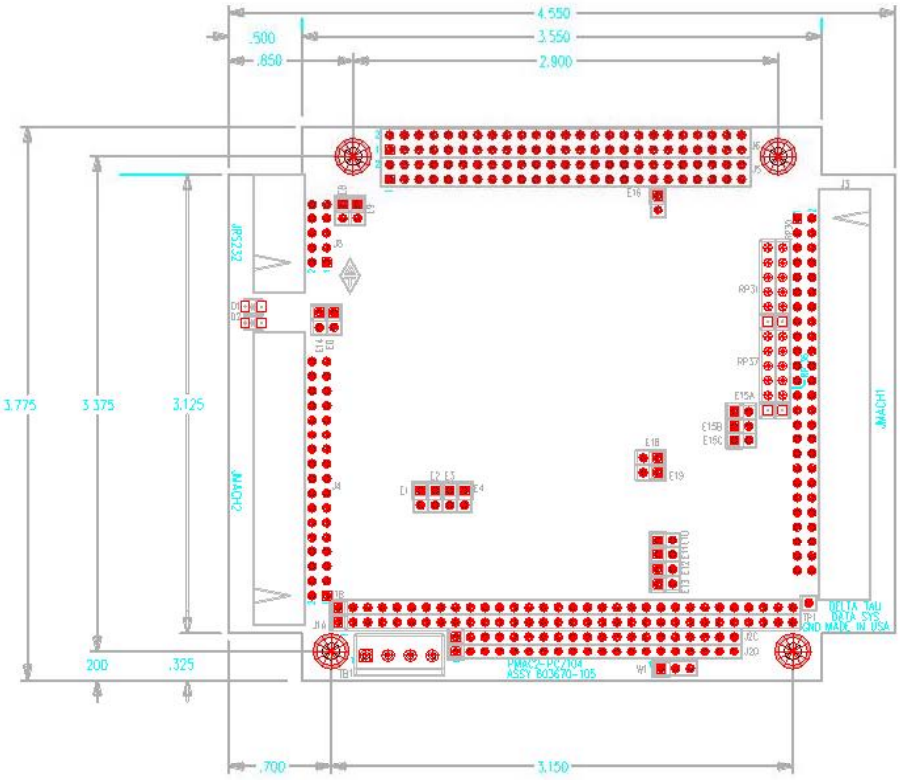
HARDWARE REFERENCE SUMMARY

The following information is based on the PMAC2A PC/104 board, part number 603670-100.

Board Dimensions

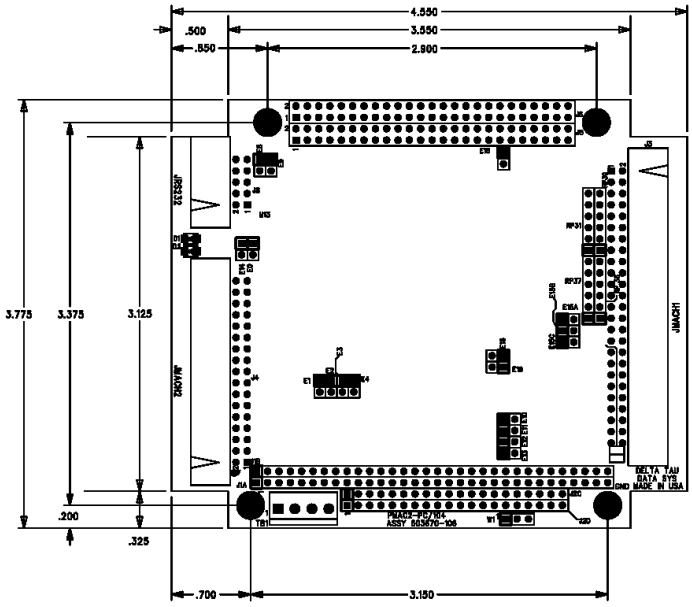
From v106 to 107

(E20-23 added and 15A is in a different location:



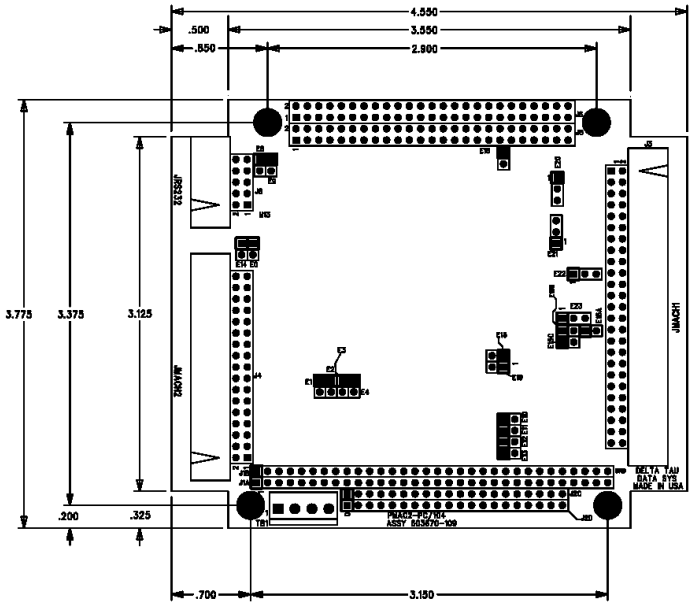
From v107 to 108

W1 removed:



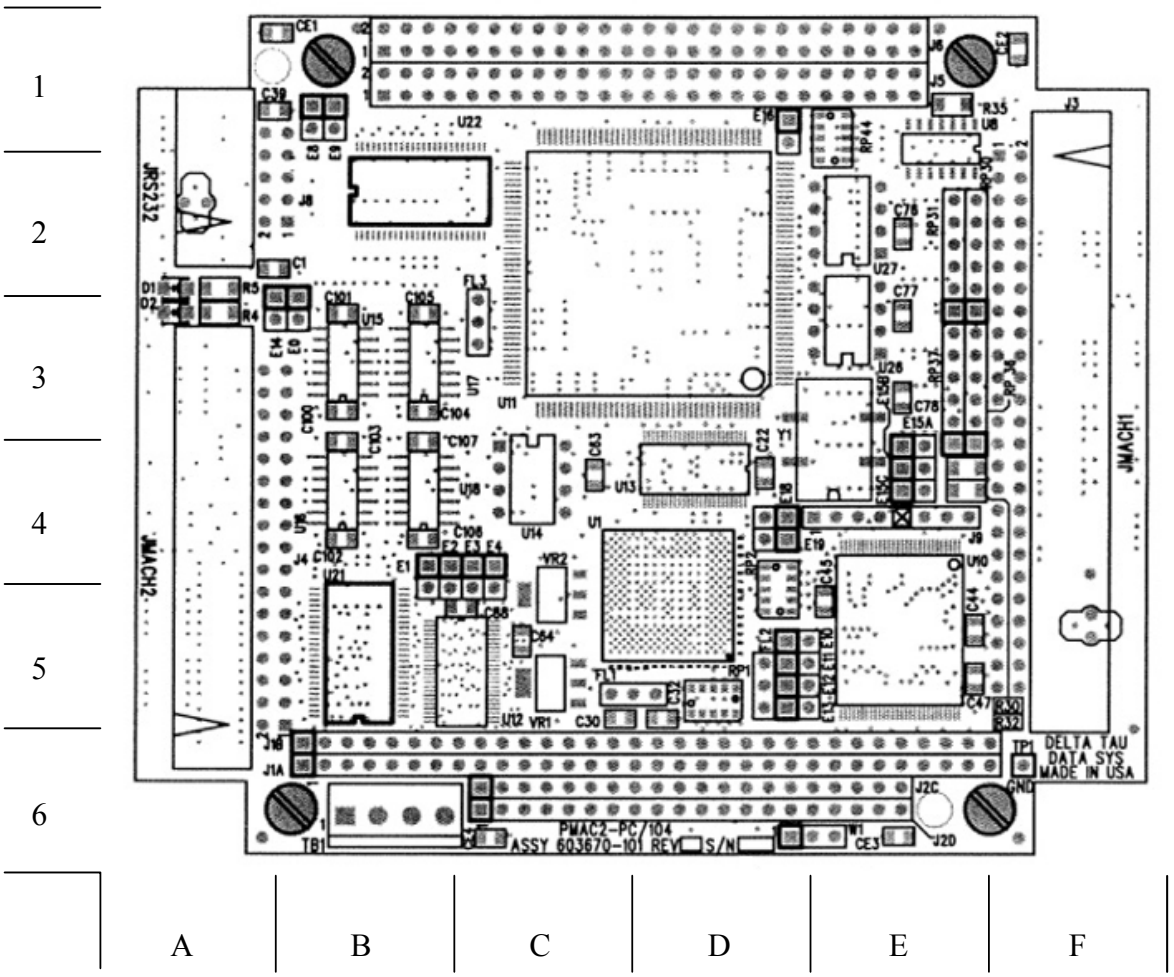
From v108 to 109

E20 in same location but rotated 90 degrees:



603670-9manual.pcb – Fri Jul 28 13:45:31 2006

Board Layout



Feature	Location	Feature	Location	Feature	Location
E0	B3	**E13**	E5	**RP30**	E2
E1	B4	**E14**	B3	**RP31**	E2
E2	B4	**E15A**	E4	**RP36**	E3
E3	C4	**E15B**	E4	**RP37**	E3
E4	C4	**E15C**	E4	**D1**	A2
E8	B1	**E16**	D1	**D2**	A3
E9	B1	**E18**	D4	**TB1**	B6
E10	E5	**E19**	D4	**JRS232**	A2
E11	E5	**W1**	E6	**JMACH1**	F3
E12	E5			**JMACH2**	A4

Connectors and Indicators

J3 - Machine Connector (JMACH1 Port)

The primary machine interface connector is JMACH1, labeled J3 on the PMAC. It contains the pins for four channels of machine I/O: analog outputs, incremental encoder inputs, amplifier fault and enable signals and power-supply connections.

1. 50-pin female flat cable connector T&B Ansley P/N 609-5041
2. Standard flat cable stranded 50-wire T&B Ansley P/N 171-50
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9

J4 - Machine Connector (JMACH2 Port)

This machine interface connector is labeled JMACH2 or J4 on the PMAC. It contains the pins for four channels of machine I/O: end-of-travel input flags, home flag and pulse-and-direction output signals. In addition, the B_WDO output allows monitoring the state of the Watchdog safety feature.

1. 34-pin female flat cable connector T&B Ansley P/N 609-3441
2. Standard flat cable stranded 34-wire T&B Ansley P/N 171-34
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J8 - Serial Port (JRS232 Port)

This connector allows communicating with PMAC from a host computer through a RS-232 port. Delta Tau provides the Accessory 3L cable that connects the PMAC to a DB-9 connector.

1. 10-pin female flat cable connector T&B Ansley P/N 609-1041
2. Standard flat cable stranded 10-wire T&B Ansley P/N 171-10

TB1 – Power Supply Terminal Block (JPWR Connector)

In almost in all cases the PMAC2A PC/104 will be powered from the PC/104 bus, when it is installed in a host computer's bus, or from the JMACH1 connector. This terminal block may be used as an alternative power supply connector or to easily measure the voltages applied to the board.

1. 4-pin terminal block, 0.150 pitch

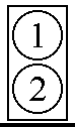
LED Indicators

D1: when this red LED is lit, it indicates that the watchdog timer has tripped and shut down the PMAC.

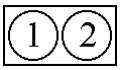
D2: when this green LED is lit, it indicates that power is applied to the +5V input.

E-POINT JUMPER DESCRIPTIONS

E0: Forced Reset Control

E Point and Physical Layout	Location	Description	Default
E0 	B3	Factory use only; the board will not operate with E0 installed.	No jumper

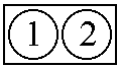
E1: Servo and Phase Clock Direction Control

E Point and Physical Layout	Location	Description	Default
E1 	B4	Remove jumper for PMAC to use its internally generated servo and phase clock signals and to output these signals on the J8 serial port connector. Jump pins 1 and 2 for PMAC to expect to receive its servo and phase clock signals on the J8 serial port connector.	No jumper installed

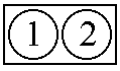
Note:

If the E1 jumper is ON and the servo and phase clocks are not brought in on the J8 serial port, the watchdog timer will trip immediately.

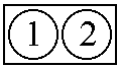
E2: CPU Frequency Select

E Point and Physical Layout	Location	Description	Default
E2 	B4	Remove jumper for 40 MHz operation (E4 OFF also) or for 80 MHz operation (E4 ON). Jump pin 1 to 2 for 60 MHz operation (E4 OFF).	No jumper installed

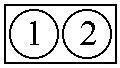
E3: Normal/Re-Initializing Power-Up/Reset

E Point and Physical Layout	Location	Description	Default
E3 	C4	Jump pin 1 to 2 to re-initialize on power-up/reset, loading factory default settings. Remove jumper for normal power-up/reset, loading user-saved settings.	No jumper installed

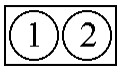
E4: CPU Frequency Select

E Point and Physical Layout	Location	Description	Default
E4  	C4	Remove jumper for 40 MHz operation (E2 OFF also) or for 60 MHz operation (E4 ON). Jump pin 1 to 2 for 80 MHz operation (E2 OFF).	No jumper installed (standard or Option 5EF) Jumper installed (Option 5CF)

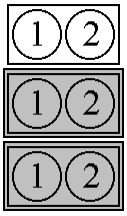
E8: Phase Clock Lines Output Enable

E Point and Physical Layout	Location	Description	Default
E8  	B1	Jump pin 1 to 2 to enable the PHASE clock line on the J8 connector, allowing synchronization with another PMAC. Remove jumper to disable the PHASE clock line on the J8 connector.	No Jumper

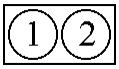
E9: Servo Clock Lines Output Enable

E Point and Physical Layout	Location	Description	Default
E9  	B1	Jump pin 1 to 2 to enable the SERVO clock line on the J8 connector, allowing synchronization with another PMAC. Remove jumper to disable the SERVO clock line on the J8 connector.	No Jumper

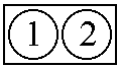
E10 – E12: Power-Up State Jumpers

E Point and Physical Layout	Location	Description	Default
E10  **E12**	E5	Remove jumper E10; Jump E11; Jump E12; To read flash IC on power-up/reset Other combinations are for factory use only; the board will not operate in any other configuration.	No E10 jumper installed; Jump E11 and E12

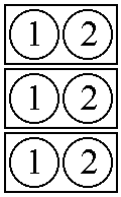
E13: Power-Up/Reset Load Source

E Point and Physical Layout	Location	Description	Default
E13  	E5	Jump pin 1 to 2 to reload firmware through serial or bus port. Remove jumper for normal operation.	No jumper

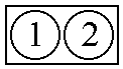
E14: Watchdog Disable Jumper

E Point and Physical Layout	Location	Description	Default
E14  	B3	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper

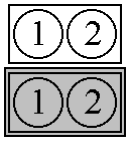
E15A, B, C: Flash Memory Bank Select

E Point and Physical Layout	Location	Description	Default
E15A  **E15C**	E4	Remove all 3 jumpers to select flash memory bank with factory-installed firmware. Use other configuration to select one of the 7 other flash memory banks.	No jumpers installed

E16: ADC Inputs Enable

E Point and Physical Layout	Location	Description	Default
E16  	D1	Jump pin 1 to 2 to enable the Option-12 ADC inputs. Remove jumper to disable the ADC inputs, which might be necessary for reading current feedback signals from digital amplifiers.	No jumper

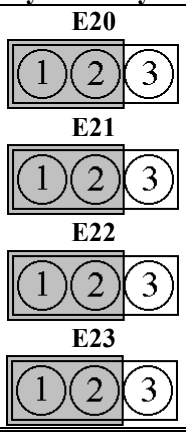
E18 – E19: PC/104 Bus Address

E Point and Physical Layout	Location	Description				Default
	D4	Jumpers E18 and E19 select the PC/104 bus address for communications according to the following table:				No E18 jumper installed; Jumper E19 installed
		E18	**E19**	**Address (Hex)**	**Address (Dec)**	
		OFF	OFF	$200	512	
		OFF	ON	$210	528	
		ON	OFF	$220	544	
		ON	ON	$230	560	

Note:

Jumper E18 must be removed and jumper E19 must be installed for using either the Ethernet or USB optional methods of communication.

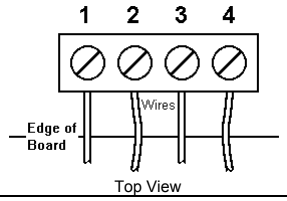
E20-E23: ENCODER SINGLE ENDED/DIFFERENTIAL SELECT (Note: v107 and above only)

E Point and Physical Layout	Location	Description	Default
		Jump pin 2 to 3 to obtain differential encoder input mode. This will bias encoder negative inputs to VCC = 5V Jump pin 1 to 2 to obtain non-differential encoder input mode. This will bias encoder negative inputs to 1/2 VCC = 2.5V	1-2 Jumper installed

CONNECTOR PINOUTS

TB1 (JPWR): Power Supply

(4-Pin Terminal Block)

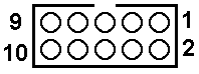


Pin#	Symbol	Function	Description	Notes
1	GND	Common	Digital Common	
2	+5V	Input	Logic Voltage	Supplies all PMAC digital circuits
3	+12V	Input	DAC Supply Voltage	Ref to Digital GND
4	-12V	Input	DAC Supply Voltage	Ref to Digital GND

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC board when it is not in a bus configuration. When the PMAC is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply; in this case, this terminal block should not be used.

J4 (JRS232) Serial Port Connector

(10-PIN CONNECTOR)

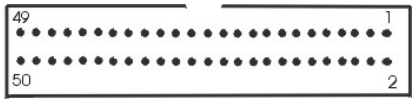


Front View

Pin#	Symbol	Function	Description	Notes
1	PHASE	Output	Phasing Clock	
2	DTR	Bidirect	Data Terminal Ready	Tied to "DSR"
3	TXD/	Input	Receive Data	Host transmit data
4	CTS	Input	Clear to Send	Host ready bit
5	RXD/	Output	Send Data	Host receive data
6	RTS	Output	Request to Send	PMAC ready bit
7	DSR	Bidirect	Data Set Ready	Tied to "DTR"
8	SERVO	Output	Servo Clock	
9	GND	Common	Digital Common	
10	+5V	Output	+5Vdc Supply	Power supply out

J3 (JMACH1): Machine Port Connector

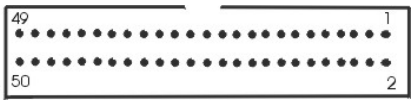
(50-Pin Header)



Top View

Pin#	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	For encoders, 1
4	GND	Common	Digital Common	For encoders, 1
5	CHA1	Input	Encoder A Channel Positive	2
6	CHA2	Input	Encoder A Channel Positive	2
7	CHA1/	Input	Encoder A Channel Negative	2,3
8	CHA2/	Input	Encoder A Channel Negative	2,3
9	CHB1	Input	Encoder B Channel Positive	2
10	CHB2	Input	Encoder B Channel Positive	2
11	CHB1/	Input	Encoder B Channel Negative	2,3
12	CHB2/	Input	Encoder B Channel Negative	2,3
13	CHC1	Input	Encoder C Channel Positive	2
14	CHC2	Input	Encoder C Channel Positive	2
15	CHC1/	Input	Encoder C Channel Negative	2,3
16	CHC2/	Input	Encoder C Channel Negative	2,3
17	CHA3	Input	Encoder A Channel Positive	2
18	CHA4	Input	Encoder A Channel Positive	2
19	CHA3/	Input	Encoder A Channel Negative	2,3
20	CHA4/	Input	Encoder A Channel Negative	2,3
21	CHB3	Input	Encoder B Channel Positive	2
22	CHB4	Input	Encoder B Channel Positive	2
23	CHB3/	Input	Encoder B Channel Negative	2,3
24	CHB4/	Input	Encoder B Channel Negative	2,3
25	CHC3	Input	Encoder C Channel Positive	2
26	CHC4	Input	Encoder C Channel Positive	2
27	CHC3/	Input	Encoder C Channel Negative	2,3
28	CHC4/	Input	Encoder C Channel Negative	2,3
29	DAC1	Output	Analog Output Positive 1	4
30	DAC2	Output	Analog Output Positive 2	4
31	DAC1/	Output	Analog Output Negative 1	4,5
32	DAC2/	Output	Analog Output Negative 2	4,5
33	AENA1/	Output	Amplifier-Enable 1	
34	AENA2/	Output	Amplifier -Enable 2	
35	FAULT1/	Input	Amplifier -Fault 1	6
36	FAULT2/	Input	Amplifier -Fault 2	6
37	DAC3	Output	Analog Output Positive 3	4
38	DAC4	Output	Analog Output Positive 4	4
39	DAC3/	Output	Analog Output Negative 3	4,5

J3 JMACH1 (50-Pin Header)
(Continued)



Top View

Pin#	Symbol	Function	Description	Notes
40	DAC4/	Output	Analog Output Negative 4	4,5
41	AENA3/	Output	Amplifier -Enable 3	
42	AENA4/	Output	Amplifier -Enable 4	
43	FAULT3/	Input	Amplifier -Fault 3	6
44	FAULT4/	Input	Amplifier -Fault 4	6
45	ADCIN_1	Input	Analog Input 1	Option-12 required
46	ADCIN_2	Input	Analog Input 2	Option-12 required
47	FLT_FLG_V	Input	Amplifier Fault pull-up V+	
48	GND	Common	Digital Common	
49	+12V	Input	DAC Supply Voltage	7
50	-12V	Input	DAC Supply Voltage	7

The J3 connector is used to connect PMAC to the first 4 channels (Channels 1, 2, 3, and 4) of servo amps and encoders.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry.

Note 2: Referenced to digital common (GND). Maximum of ±12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders).

Note 4: ±10V, 10 mA max, referenced to common ground (GND).

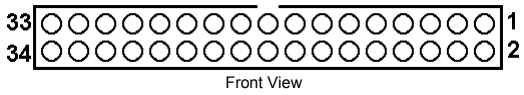
Note 5: Leave floating if not used. Do not tie to GND.

Note 6: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually GND) to produce a 0 in PMAC software. Automatic fault function can be disabled with Ix25.

Note 7: Can be used to provide input power when the PC/104 bus connector is not being used. When the bus configuratio is used, these supply voltages automatically come through the bus connector from the PC power supply.

J4 (JMACH2): Machine Port CPU Connector

(34-Pin Header)



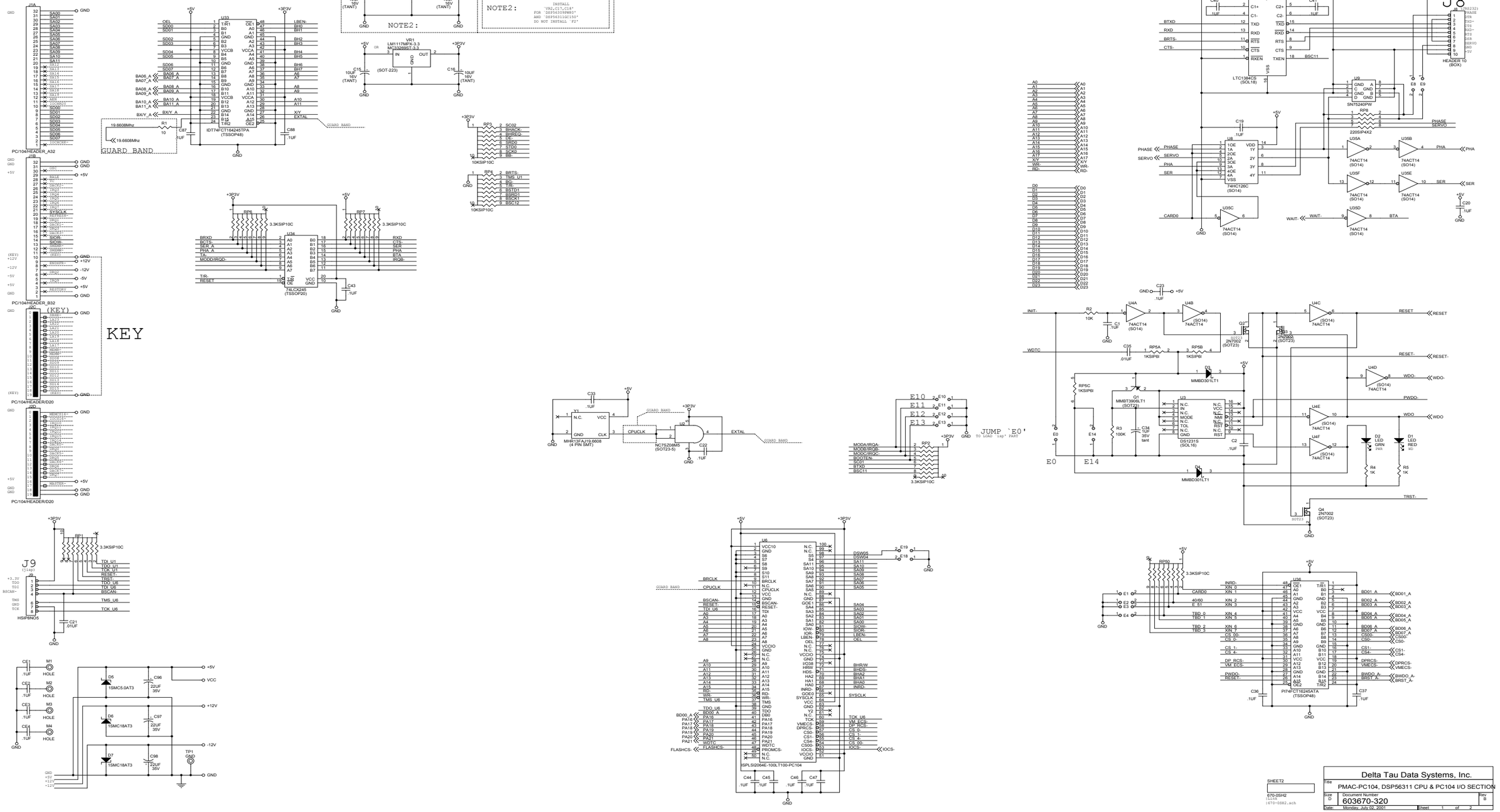
Pin#	Symbol	Function	Description	Notes
1	FLG_1_2_V	Input	Flags 1-2 Pull-Up	
2	FLG_3_4_V	Input	Flags 3-4 Pull-Up	
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	HOME1	Input	Home-Flag 1	10
6	HOME2	Input	Home-Flag 2	10
7	PLIM1	Input	Positive End Limit 1	8,9
8	PLIM2	Input	Positive End Limit 2	8,9
9	MLIM1	Input	Negative End Limit 1	8,9
10	MLIM2	Input	Negative End Limit 2	8,9
11	USER1	Input	User Flag 1	
12	USER2	Input	User Flag 2	
13	PUL_1	Output	Pulse Output 1	
14	PUL_2	Output	Pulse Output 2	
15	DIR_1	Output	Direction Output 1	
16	DIR_2	Output	Direction Output 2	
17	EQU1	Output	Encoder Comp-Equal 1	
18	EQU2	Output	Encoder Comp-Equal 2	
19	HOME3	Input	Home-Flag 3	10
20	HOME4	Input	Home-Flag 4	10
21	PLIM3	Input	Positive End Limit 3	8,9
22	PLIM4	Input	Positive End Limit 4	8,9
23	MLIM3	Input	Negative End Limit 3	8,9
24	MLIM4	Input	Negative End Limit 4	8,9
25	USER1	Input	User Flag 3	
26	USER2	Input	User Flag 4	
27	PUL_3	Output	Pulse Output 3	
28	PUL_4	Output	Pulse Output 4	
29	DIR_3	Output	Direction Output 3	
30	DIR_4	Output	Direction Output 4	
31	EQU3	Output	Encoder Comp-Equal 3	
32	EQU4	Output	Encoder Comp-Equal 4	
33	B_WDO	Output	Watchdog Out	Indicator/driver
34	No Connect			

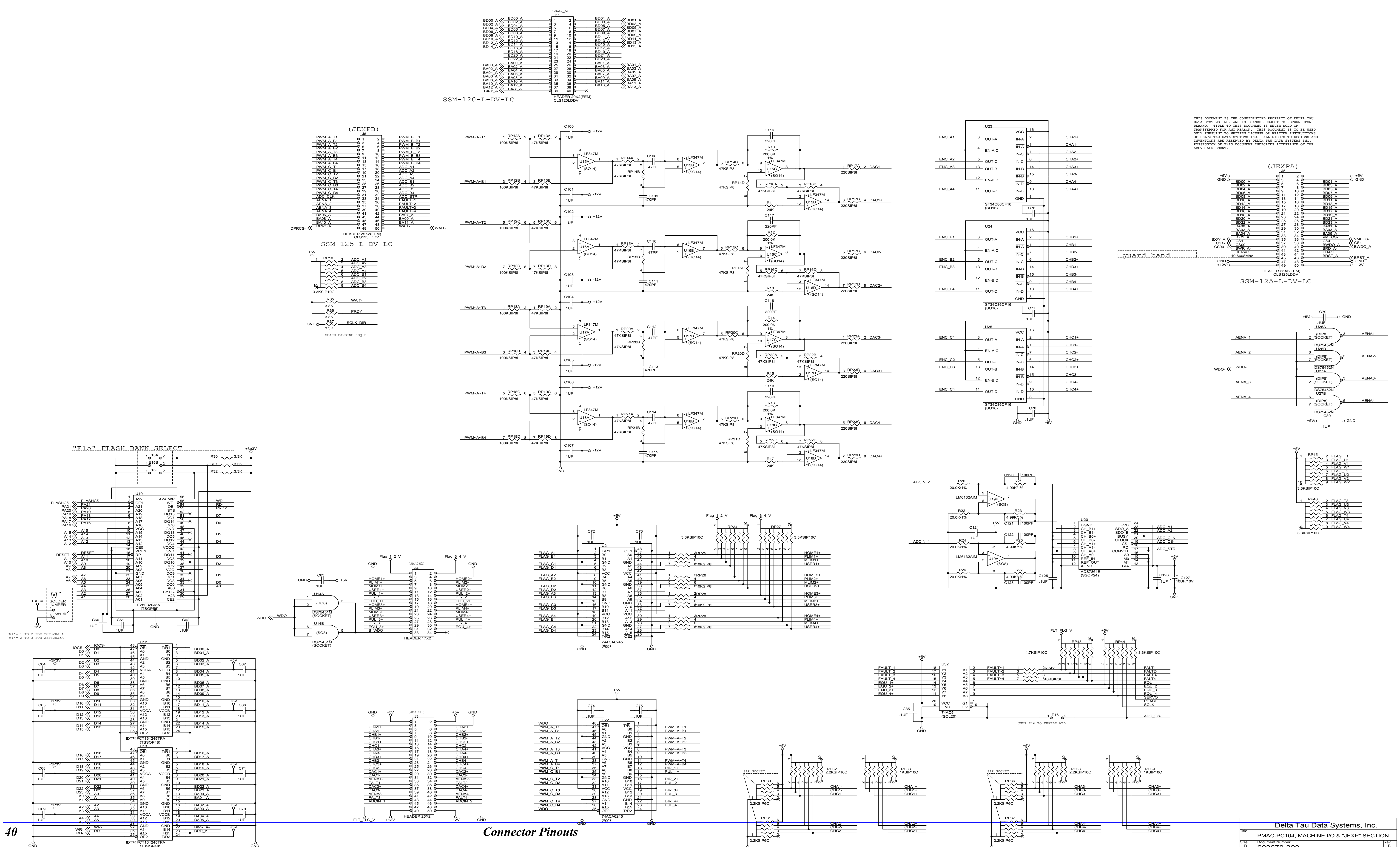
Note 8: Pins marked *PLIMn* should be connected to switches at the *positive* end of travel. Pins marked *MLIMn* should be connected to switches at the *negative* end of travel.

Note 9: Must be conducting to 0V (usually GND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HOMEn controlled by Encoder/Flag Variable I9n2. HMFLn selected for trigger by Encoder/Flag Variable I9n3. Must be conducting to 0V (usually GND) to produce a 0 in PMAC software.

SCHEMATICS




(JEXP_A)
SSM-120-L-DV-LC
HEADER 20X2(FEM)
CLS120LDDV
(JEXPB)
HEADER 25X2(FEM)
CLS125LDDV
SSM-125-L-DV-LC
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(JEXPA)
guard band
SSM-125-L-DV-LC
"E15" FLASH BANK SELECT
W1
SOLDER JUMPER
E28F320J3A
(TSSOP56)
`W1'= 1 TO 2 FOR 28F320J3A
`W1'= 2 TO 3 FOR 28F320J5A
IDT74FCT164245TPA
(TSSOP48)
(JMACH2)
HEADER 17X2
(JMACH1)
HEADER 25X2
74ACA6245
(dgg)
ADS7861E
(SSOP24)
74AC541
(SOL20)
JUMP E16 TO ENABLE ATD
SIP SOCKET
670-0SH2.sch
Delta Tau Data Systems, Inc.
Title
PMAC-PC104, MACHINE I/O & "JEXP" SECTION
Size
D
Document Number
603670-320
Rev
B
Date: Monday, July 02, 2001
Sheet 2 of 2